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Area Delay Power Efficient and Implementation of Modified Square-Root Carry Select Adder Architecture

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Abstract: In VLSI Technology, Carry Propagation Delay is the most important concern for the Adders. Adder is the most unavoidable component for the arithmetic performances. This paper is Modified Square Root-Carry Select Adder (SQRT-CSLA) design reduces the delay with 16 bit adder. Carry select adder have two units for Carry Generation (CG) and Carry Selection (CS). The modified SQRT-CSLA design can gives parallel path for carry propagation. So the overall adder delay has reduced. Modified design is obtained using Ripple Carry Adder (RCA) with Boolean Excess-1 Converter (BEC). BEC produces an output i.e., is an excess one result for given input bits. Then input bits and BEC output is given to multiplexer for carry selection. Use of BEC instead of dual RCA gives efficient carry propagation delay and it consumes the lower power and overall gates using in design is reduced with compared to carry select adder with dual RCA. The final sum is calculated using final sum generation.

Index Terms: RCA, BEC with MUX and Modified SQRT-CSLA

I.INTRODUCTION

In the VLSI technology, the low power adder circuits are widely used due to their fast and increase of convenient electronics component. A speedy operation of a digital system is generally influenced by the tenant adders. The most important and widely accepted metrics for measuring the quality of adder designs are power, delay and area. Optimizing the area, delay has always been considered an important for VLSI design stipulation. Then the reduction of power dissipation has come to for as a major design goal aspect. Here digital adders, the speed of addition are limited by the time required to propagate a carry through the adder. High-speed addition and multiplication has always been a fundamental requirement of high- performance processors and systems.

The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and carries propagated into the next block. The major problem of main speed limitation in several adders is in generation of carries. This speed limitation can be conquering by using carry select adder (CSLA) and this CSLA is a fastest adder among all other adders. Then CSLA has mainly two types i.e., square-root and linear. Here uses a CSLA with square-root type and it are an efficient and fast adder.

II.RIPPLE CARRY ADDER

A ripple carry (RCA) adder is a digital circuit that gives the two binary values while performing arithmetic summation. It can be builds with two full adder blocks connected in parallel form and it produces carry output from each full adder blocks connected to the next full adder block to gives the carry input. RCA is one of the types of adder to use of arithmetic functions and it used in first stage of this paper.

A.2-Bit Ripple Carry Adders

In this project, uses a two-bit ripple carry adder and RCA consists of two full adders (FA) block in it. 2-bit RCA structure is shown in figure 1. After that, 2-bit binary inputs and Cin=1 are given to the two full adders. Then, the sum and carry are generated by first full adder block. This carry is propagates through the next full adder block, after only starts to addition process and it will also generates the sum and carry. These results are given to the new modified Square Root-Carry Select adder (SQRT-CSLA).

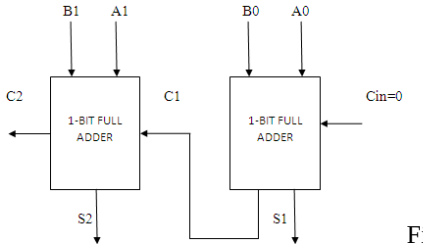

Fig 1:
Construction of Two-bit full adder

III. FULL ADDER

A full adder is a adder circuits and it contains two half adders. FA can perform the addition of three input bits and gives the result of sum and carry. The three input bits are A, B and C_{in} and the output of Sum and C_{out}. The full adder is shown in following figure 2.

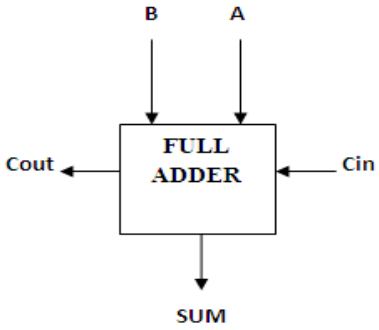

Fig 2: Structure of full adder

IV.BINARY EXCESS-1 CONVERTER

The use of binary to excess-1 code converter is to converts binary value into excess one form of binary representation. In this project, dual pair RCA is replaced by BEC in the new modified SQRT-CSLA architecture to get lower area and improved speed of performance than RCA. Because of high propagation delay was produced when generating partial sum and carry due to the use of dual RCA pair. The gate counts are used in this modified CSLA gets reduced.

A. Binary Excess Code

The modified Square root Carry select adder has a single ripple carry adder with Binary to Excess-I converter, which replace the ripple carry adder with Cin=l, in order to reduce the area and power consumption of the regular CSLA. Here n+1 BEC is used instead of n-bit RCA. Table I shows the 4-bit BEC.

Table I: Binary to Binary excess-1 code conversion

Binary value[3:0]	Binary excess-1 code[3:0]
0000	0001
0001	0010
0010	0011
0011	0100
.	.
.	.
.	.
1111	0000

B.BEC with Mux

The BEC is constructed with Multiplexer (MUX) circuit and here shows a BEC with 8:4 MUX in figure 3. One input of the 8:4 MUX gets as it input (B3, B2, B1, and B0) and another input of the MUX is the BEC output. This structure can possibly generate parallel two results and the MUX is selecting either the BEC output or straight input based on the control signal cin. The significance of the BEC logic is from the large area reduction when designing of CSLA with large binary numbers.

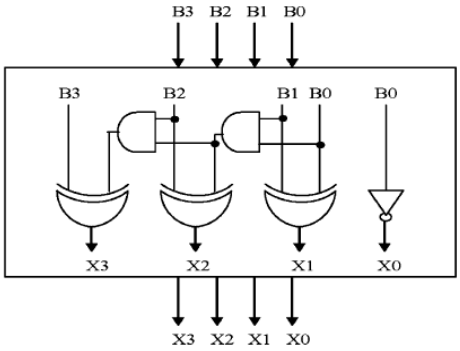

Fig 3: BEC logic with MUX

V.REGULAR CSLA

In this method n-bit input are given to the first Ripple carry adder (RCA) block with Cin of 0 and it produces a sum and carry. After getting carry only, the second RCA block will start to process on Cin of 1. Until, this second RCA get carry from previous block, it will wait to get. So those, the problem were increased in delay and power. And after that, the right sum and carry is selected in the selection unit. This regular CSLA method is shows in figure 4.

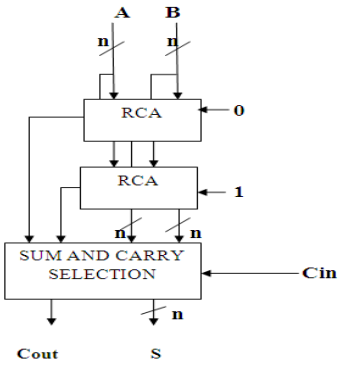

Fig 4: Regular CSLA structure

VI.NEW MODIFIED SQRT-CSLA

The Binary to excess one Converter (BEC) used instead of the RCA with signal input cin=1 because of reduce the area and power utilization of the regular CSLA. The new modified 16-bit SQRT-CSLA using BEC is shown in figure 4. Then the structure is further divided into five major blocks with RCA and BEC.

One input to the MUX goes from the RCA with Cin=0 and other input from the BEC. Clearly gives best result about the BEC structure reduces the number of gate counts used in the design and less power consumption compares to the regular CSLA.

VII. SIMULATION RESULTS AND IMPLEMENTATION

The regular SQRT-CSLA and new modified 16-bit SQRT-CSLA experimental results are given in following below fiure 5 and figure 6. Comparison results of the regular SQRT-CSLA and new modified 16-bit SQRT-CSLA is given in table II.

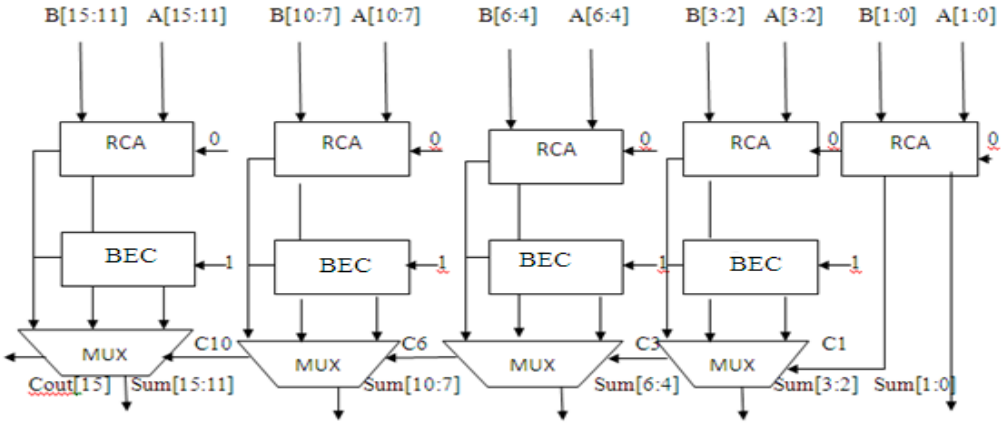

Fig 5: New modified 16-bit SQRT-CSLA

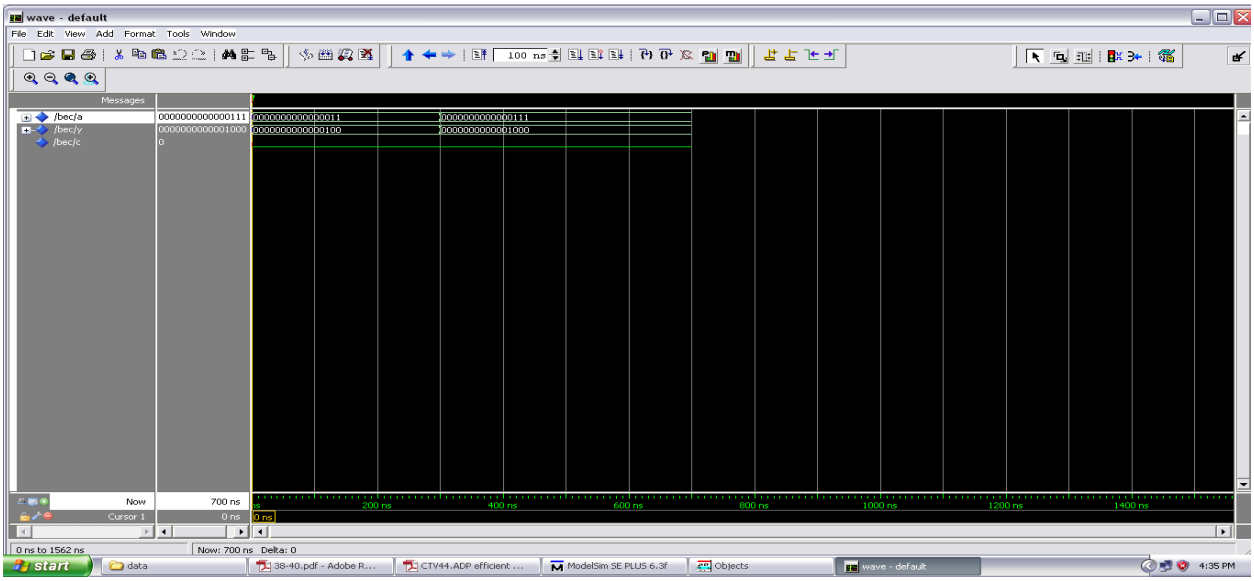

Fig 6: Simulation result of regular CSLA

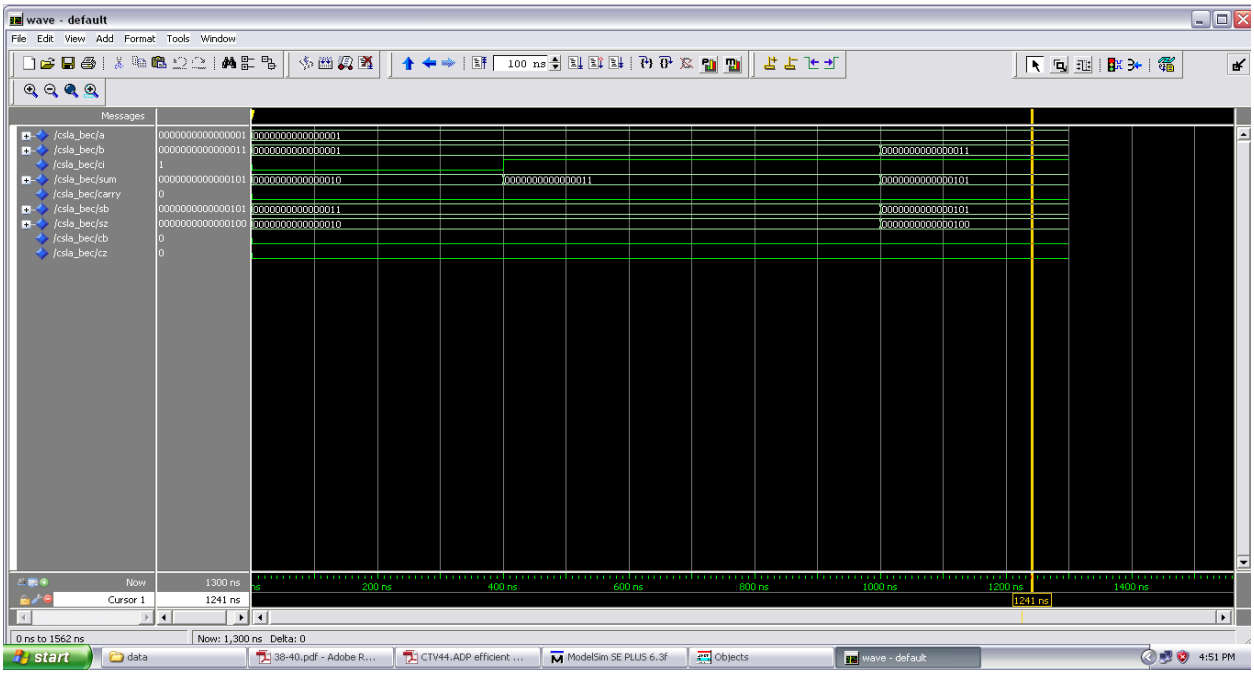

Fig 7: simulation result of new modified SQRT-CSLA

Table II: Area, delay results compared with conventional method

DESIGN	GATE COUNIS	POWER(mW)	DELAY(ns)
Regular SQRT-CSLA	348	97	28.281
NEW MODIFIED SQRT-CSLA	248	72	25.209

VIII. CONCLUSION

In this paper, the new 16-bit modified square root carry select adder designed replacement of ripple carry adder by binary to excess one converter (BEC) in existing method. VHSIC Hardware Description Language (VHDL) codes are done by use of Xilinx ISE 8.1i/ Modelsim SE 6.5 and simulation waveform and design reports are clearly indicating this design is an efficient to lesser delay and power. Modified SQRT-CSLA design gives an efficient and fast carry select adder than the existing adder because of this design produced overall delay of 25.209 ns, power of 72 ns and the total logic gates are used in design to 248 gate counts.

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