INTERNATIONAL JOURNAL FOR TRENDS IN ENGINEERING & TECHNOLOGY,
VOLUME 3 ISSUE 2 – FEBRUARY 2015 – ISSN: 2349 – 9303

Diode Free T-Type Five Level Neutral Point Clamped Inverter for Low Voltage Dc System

Krishna KC[1]
[1]Hinduthan College of Engineering & technology,
Department of Applied electronics,
Krishnakc2311@gmail.com

M.P.Viswanathan[2]
[2]Hinduthan College of Engineering & Technology,
Department of electrical and electronic,
viswaveena@gmail.com

Abstract—The multilevel inverter is used as a solution to increase the inverter operating voltage above the voltage limits of classical semiconductors. A Diode Free T-Type Five Level NPC inverter for Low Voltage DC System is proposed in this paper. The T-Type inverter topology is more efficient and conventional than I-type inverter topology. Considerable suppression of the harmonic current is the ultimate goal of multilevel inverter. Losses like Semiconductor loss, conduction loss are mainly due to IGBT & diode in the current path. So the proposed system is designed with cool MOSFET without diode. The middle bidirectional switch is replaced by two pair of MOSFET. Hence the five level NPC inverter is more significant for low and medium power range DC source and for Renewable energy system.

Index Terms— NPC, COOLMOSFET, Power Factor, Total Harmonic Distortion, Harmonic current

1 INTRODUCTION

THE power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. batteries ,Capacitors, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. On using multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. Multilevel inverters offer various applications in voltage r anging from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. The multilevel starts from three levels, as the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero.

Mostly cascaded multilevel inverter is used due to it ease of deign. H bridge type of multilevel was later used. Then clamped type of inverter was implemented. In the clamped type inverter the clamping is done by diode, capacitor and by neutral clamping method.

The main objective of multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, which are typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion[20].

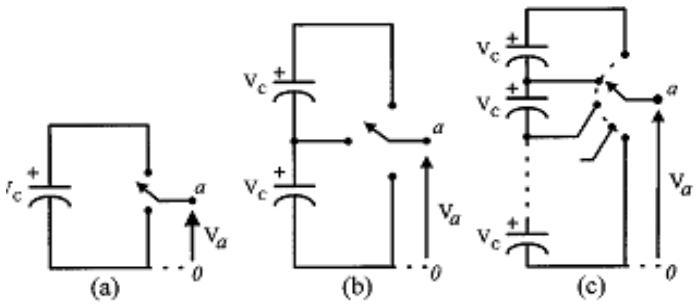

Figure 1 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

In Figure 1(a) the output Va can take values i.e. 0 and V c as possible values. In Figure 1(b) the output Va can take three possible values i.e. 0,Vc and 2Vc . In Figure 1(c) the output Va can take four possible values i.e. . 0, Vc , 2Vc and 3Vc.It can be extended further. The number of possible outputs presents the level of the inverter that is shown in figure 2.

1.1 Neutral point clamped inverter (NPC)

The neutral point clamped topology is also known as diode clamped topology. The main advantage of the NPC topology is that it

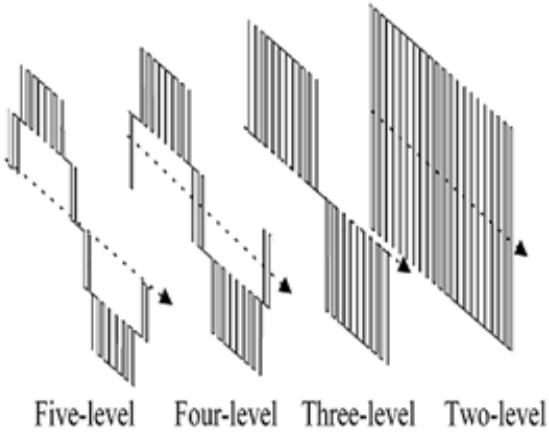

Figure 2 Waveforms of Multilevel inverter

-requires only one DC source similar to two-level inverter, and gives better performance. With the increase in level 'n', not only the number of clamping diodes increases but also the problem of ensuring the DC-link balance becomes more severe. Due to these reasons, the NPC topology is mainly used for 3- level inverter. Figure 3 shows its 3-level NPC topology.

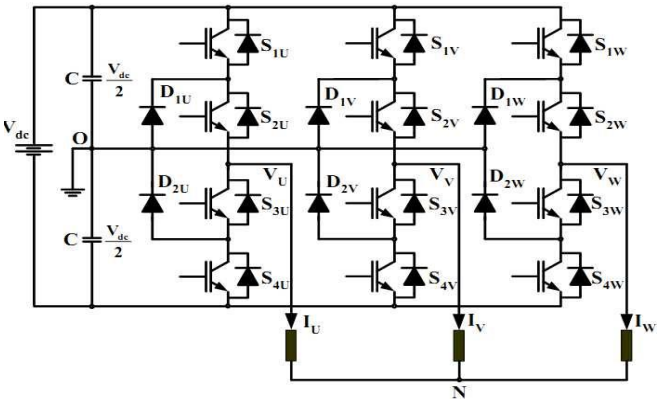

Figure 3 Three -level Neutral Point Clamped topology

2 INVESTIGATION 5L-NPC INVERTER FOR LOW VOLTAGE DC SYSTEM

Currently, I-type 5L-NPC has been studied and applied dominantly in low-voltage DC systems [12], [13].The authors in [14] proposed a three-level active clamped NPC inverter used for renewable energy systems to improve the efficiency. The 3L-NPC wind converter's operation strategy under unbalanced grid condition is discussed in [15]. The authors in [16] proposed a split inductor I-type 3L-NPC in the solar system for low leakage current and dead-time elimination. A novel highly efficient stacked 3L-NPC (3L-SNPC) inverter is proposed in [17] to provide the paralleled current paths. Based on the work in [17], the authors in [18] proposed an active clamped 3L-SNPC to further distribute power losses evenly.

- *Krishna KC is currently pursuing master's degree program in Applied Electronics in Hindusthan college of engineering & technology, Coimbatore, .*
E-mail: krishnakc2311@gmail.com

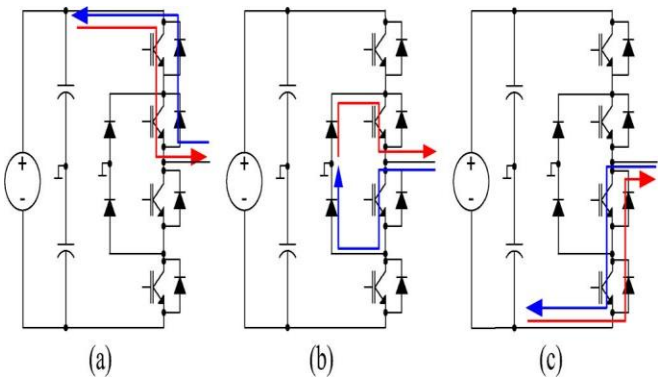

Figure 4 Current paths of conventional I-type 3L-NPC leg. (a) 1100. (b) 0110. (c) 0011.

The aforementioned literature covers the different perspectives of I-type 3L-NPC. However, all hardware topologies are based on or derived from the fundamental I-type 3L-NPC leg, shown in Figure 3.It is worthy of noting that the renewable energy system is usually operating in a much lower power range than the rated power. Moreover, the foregoing discussed drawbacks of I-type 3L-NPC seem more prominent because of the IGBT and diode relatively larger state voltage/current ratio at the low and medium powers.

It is shown in Fig. 2 that, in both zero vector and nonzero vector, the current paths include two power devices. These long current paths imply the high conduction loss. Second, higher stray inductance, due to the long current paths, results in higher power loss and turns off over voltages.

Based on the foregoing recognitions, the T-type 3L-NPC, as shown in Figure 4, is being studied increasingly to improve the system efficiency. The authors in [10] evaluated the power loss and control scheme of T-type 3L-NPC applied in the low- voltage renewable energy system. The authors in [11] applied T-type 3L-NPC in a solar system to avoid the high conduction loss.

3 PROPOSED DIODE FREE T-TYPE 5L-NPC INVERTER AND ITS PWM STRATEGY

- The proposed diode free T-type 5L-NPC inverter for low-voltage renewable energy systems is shown in Figure In this new topology, two 600-V CoolMosfets in the reverse serial connection, replaces the IGBT + diode bidirectional middle switch in the conventional T-type 5L-NPC.
- Thus, in this topology, four Cool-Mosfets form a parallel current path to reduce the equivalent ON-state resistance. More importantly, the zero-vector current flows through two CoolMosfets in the reverse connection; hence, no body diode is involved in the current path even with the non-unity power factor.

The circuit design of proposed system is shown in the Figure 7. In this a low voltage DC source is connected to the inverter supply side. A cumulative pair of four switches is placed in t-type inverter topology. The middle point of the cool MOSFET switch pair N can be defined as the neutral point. The staircase voltage synthesis can be explained as, the neutral point n is considered as the output phase

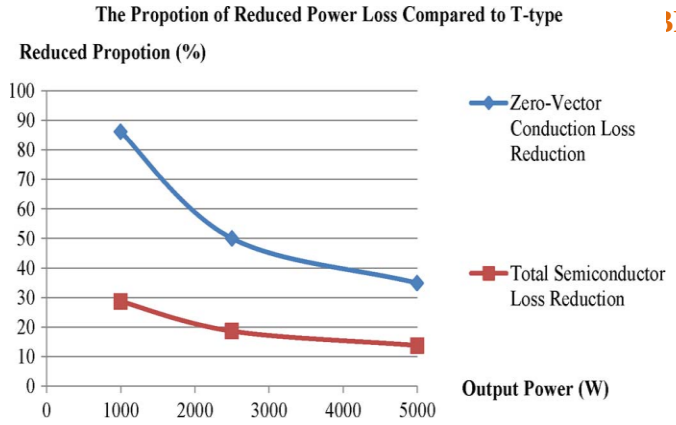

Figure 5 conduction and semiconductor loss reduction

voltage reference point four complementary switch pairs exist in each phase. By turning on one of the switches will exclude the other from being turned on this type of switch is called as complementary pair switch. The diode free neutral point clamping becomes the most convenient way for designing high-voltage high-power applications without the clamping diode.

The PWM strategy for the new topology is shown in Figure 6.With the new PWM strategy, the corresponding topological states is with the unity power factor. The current commutation within the reactive power generation region is shown in Figure 6. Here six pulses are generated for the switching the cool MOSFET in the 5l-NPC.

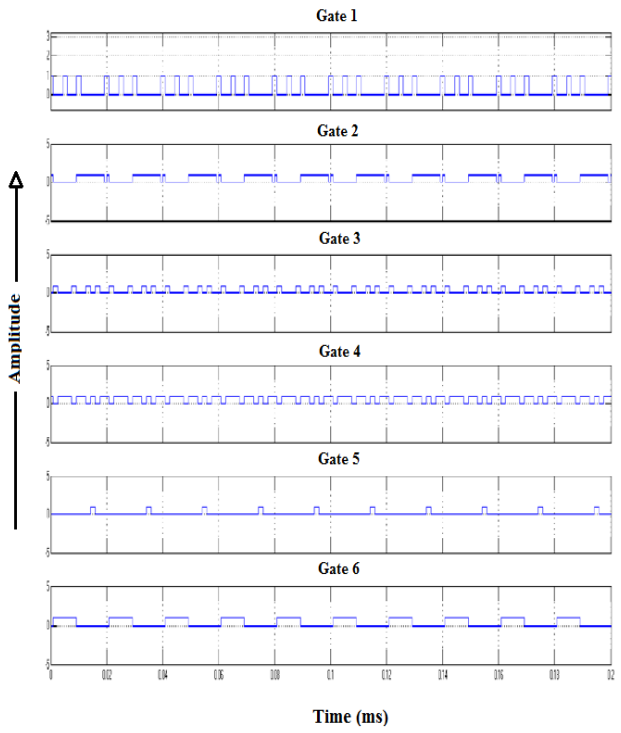

Figure 6 PWM signal

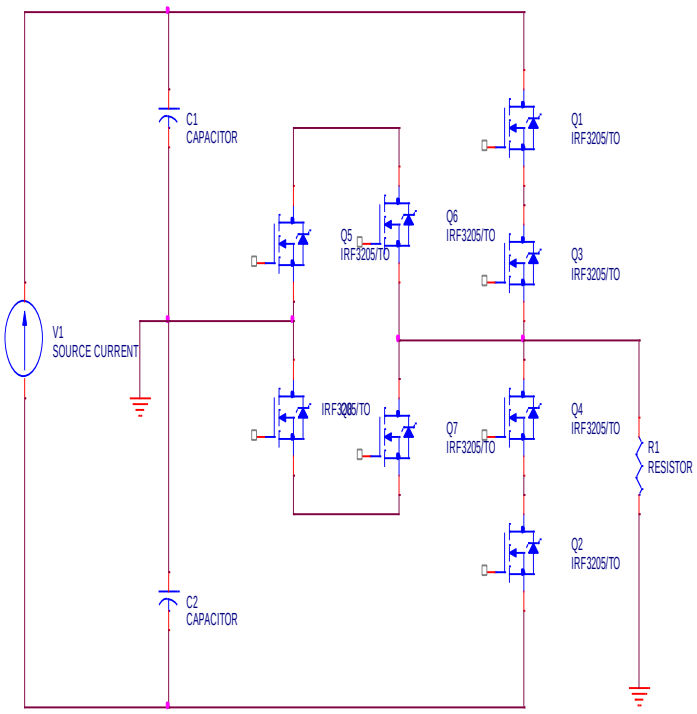

FIGURE 7 PROPOSED CIRCUIT DIAGRAM

4 RESULT AND DISCUSSION

The figure 8 shows the five level inverter output. The MOSFET switches the voltage level step by step to attain five level waveform with reduced harmonic distortion (THD=0.346). From the figure 8, it is clear that the output is continuous in the succeeding cycles. On increasing the levels the THD of the system will be reduced.

TABLE 1.1 POWER DEVICE COST EVALUATION

Type	Comment	Part number	Quantity	Price
Conventional T	IGBT	IKW40N120H3	2	3.1$
	IGBT+Diode	FGH40N60	2	1.6$
Conventional T with Mosfet+Diode	IGBT	IKW40N120H3	2	3.1$
	Mosfet	FCH104N60F	2	2.2$
	Diode	DSEP60-06A	2	1.8$
Novel T with Coolmos	IGBT	IKW40N120H3	2	3.1$
	CoolMos	SPW47N60C3	4	3.8$

The above table defines the cost of devices used for both I type and for T type inverter. On reducing the number of switches the cost of system will be reduced. In the proposed system the 5-level NPC inverter consists of one bidirectional and four switches.

In this contra flow current is totally negotiated by Mosfet. So that the system do not sufferer from component stress, the cost of the system is tolerable when compared with 3l-NPC. Hence the I–type of system will cost high so the T-type is preferred.

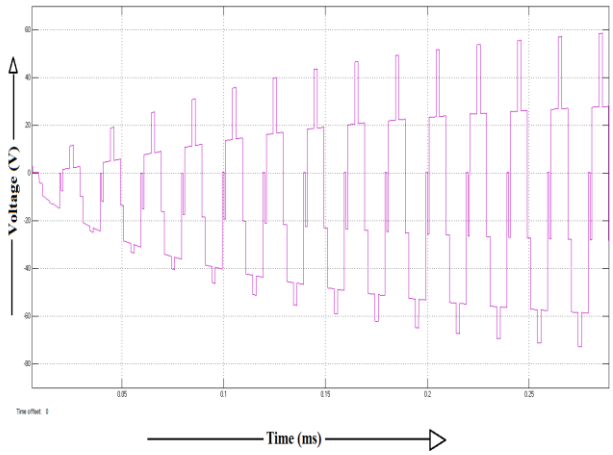

Figure 5 Inverter Side Output Voltage

The total harmonic distortion of 5level NPC inverter with diode is defined in the below figure 8.The THD of 5-l NPC with the cool Mosfets is shown in figure it define that the harmonic loss due to long conduction is reduced and the THD is also reduced to a tolerable level.

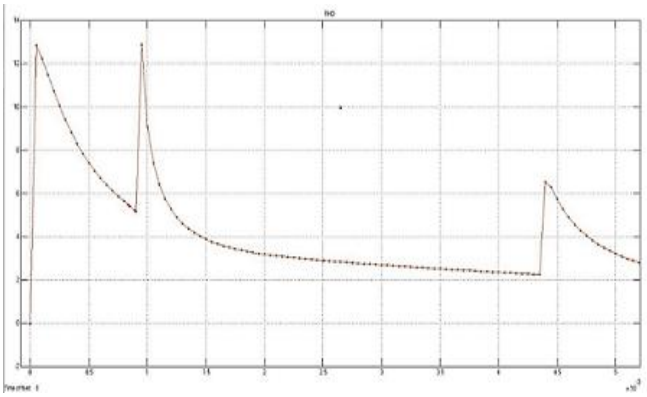

Figure 6 THD of diode switched of 5l-NPC

The system with cool Mosfet switch provide limited conduction path, due to elimination of diode in the conduction path results in short conduction path with zero vector clamping voltage. The THD waveform of diode free T-type 5l-NPC inverter is shown in figure 10

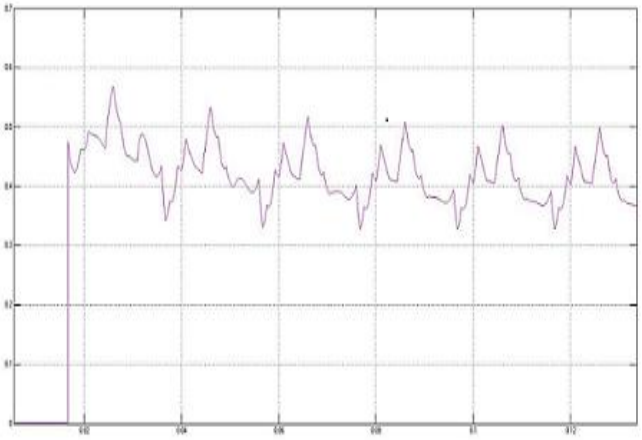

Figure 7 THD of MOSFET switched of 5l-NPC

5 CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. Multi-level PWM inverters, (including five-level inverters) have significant operational advantage, such as the ability to drive a motor with nearly sinusoidal current waveforms and at higher output voltages. The multilevel inverter topology can overcome some of the limitations of the conventional three-level inverter. Output voltage and power increase with number of levels. Harmonics decreases as the number of levels increase. In addition, increasing output voltage does not require an increase in voltage rating of individual force commutated devices. Recently, active schemes of inverter topologies and PWM strategies have been introduced in several literatures for both two-level and multi-level inverters to reduce or even eliminate common-mode voltage.

There are many multilevel inverters developed according to the voltage levels required. This project deals with the design and implementation of single-phase five-level neutral point clamped inverter. The sinusoidal PWM technique is involved in the design which has several advantages over other modulation techniques. The operational and the switching functions are analyzed in detail. In addition it is compared with the conventional three-level PWM inverter, smaller filter size, improved output waveform and other advantages.

The simulation results shows that the developed five-level PWM inverter has many merits such as

- Lower EMI,
- Less Harmonic Distortion.
- Improves the power quality and dynamic stability for utility systems.

The THD of the proposed inverter is considerably alleviated and the dynamic responses are also improved significantly.

REFERENCES

[1] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1861–1871, May 2013.

[2] R. Petrella, N. Buonocunto, A. Revelant, and P. Stocco, "DC bus volt- age equalization in single-phase split-capacitor three-level neutral-point- clamped half-bridge inverters for PV applications," in Proc. IEEE 26th Annu. APEC, Fort Worth, TX, USA, Mar. 6–11, 2011, pp. 931–938.

[3] B. P. McGrath, D. G. Holmes, and W. Y. Kong, "A decentralized controller architecture for a cascaded H-bridge multilevel converter," IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1169–1178, Mar. 2014.

[4] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single phase grid-connected converter for renewable distributed systems," IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 906–918, Mar. 2013.

[5] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multi-level con-verter topology with reduced number of power electronic components,"IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.

[6] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," IEEE Trans. Ind. Appl., vol. 41, no. 2, pp. 655–664, Mar./Apr. 2005.

[7] T. B. Soeiro and J. W. Kolar, "The new high-efficiency hybrid neutral- point-clamped converter," IEEE Trans. Ind. Electron., vol. 60, no. 5,pp. 1919–1935, May 2013.

[8] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 435–443, Jan. 2012.

[9] Y. Wang and R. Li, "Novel high-efficiency three-level stacked neutral point clamped grid tied inverter," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3766–3774, Sep. 2013.

[10] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 899–907, Feb. 2013.

[11] Y. Park, S. K. Sul, C. H. Lim, W. C. Kim, and S. H. Lee, "Asymmetric control of DC-link voltages for separate MPPTs in three-level inverters," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2760–2769, Jun. 2013.

[12] H. Abu-Rub, H. Holtz, J. Rodriguez, and B. M. Ge, "Medium-voltagemultilevel converters—State of the art, challenges, and requirements in industrial applications," IEEE Trans. Ind. Electron., vol. 57, no. 28, pp. 2581–2596, Aug. 2010.

[13] R. Gonzalez, G. Eugenio, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2694–2702, Jul. 2008.

[14] J. Li, J. J. Liu, D. Boroyevich, P. Mattavelli, and Y. S. Xue, "Three- level active neutral-point-clamped zero-current-transition converter for sustainable energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3680–3693, Dec. 2011.

[15] K. Ma, M. Liserre, and F. Blaabjerg, "Operating and loading conditions of three-level neutral-point-clamped wind power converter under various grid faults," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 520–530, Jan./Feb. 2014.

[16] H. F. Xiao and S. J. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. PowerElectron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[17] D. Floricau, G. Gateau, M. Dumitrescu, and R. Teodorescu, "A new stacked NPC converter: 3L-topology and control," in Proc. EPE, Aalborg, Denmark, Sep. 2–5, 2007, pp. 1–10.

[18] D. Floricau, G. Gateau, and A. Leredde, "New active stacked NPC multilevel converter: Operation and features," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2272–2278, Jul. 2010.

[19] A. Roshan, R. Burgos, A. C. Baisden, F. Wang, and D. Boroyevich, "A D–Q frame controller for a full-bridge single phase inverter used in small distributed power generation systems," in Proc. IEEE 22nd Annu. APEC, Anaheim, CA, USA, Feb. 25–Mar. 1 2007, pp. 641–647.

[20] T. Prathiba, P. Renuga, "A comparative study of Total Harmonic Distortion in Multi-level inverter topologies" Journal of Information Engineering and Applications, ISSN 2224-5782 ,(print) ISSN 2225-0506 (online), Vol. 2, No.3, 2012.

AUTHOR'S PROFILE

Krishna KC obtained his B.E. in Electrical and Electronics Engineering,(VEL TECH ENGINEERING COLLEGE,2013), M.E. in Applied Electronics (HINDUSTHAN COLLLEGE OF ENGG & TECHNOLOGY, 2015).He is currently doing his project work on Diode Free T-Type Five Level Neutral Point Clamped Inverter for Low Voltage DC System.

M.P.Viswanathan received his B.E. degree in Electrical and Electronics Engineering and the M.E. degree in Power Electronics and Drives. He has about 12 years of teaching experience. He is now Assistant professor in the department of Electrical and Electronics Engineering, Hindusthan College of Engineering and Technology, Coimbatore, Tamil Nadu, India. His area of interest includes Power Electronics & Drives, Digital signal processing and Digital image processing.