Diode Free T-Type Five Level Neutral Point Clamped Inverter for Low Voltage Dc System

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Abstract—The multilevel inverter is used as a solution to increase the inverter operating voltage above the voltage limits of classical semiconductors. A Diode Free T-Type Five Level NPC inverter for Low Voltage DC System is proposed in this paper. The T-Type inverter topology is more efficient and conventional than I-type inverter topology. Considerable suppression of the harmonic current is the ultimate goal of multilevel inverter. Losses like Semiconductor loss, conduction loss are mainly due to IGBT & diode in the current path. So the proposed system is designed with cool MOSFET without diode. The middle bidirectional switch is replaced by two pair of MOSFET. Hence the five level NPC inverter is more significant for low and medium power range DC source and for Renewable energy system.

Index Terms— NPC, COOLMOSFET, Power Factor, Total Harmonic Distortion, Harmonic current

1 INTRODUCTION

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Batteries, Capacitors, and renewable energy voltage sources can be used as the multiple DC voltage sources. The commutation of the power switches aggregate these multiple DC sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected.

The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. On using multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. Multilevel inverters offer various applications in voltage ranging from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. The multilevel starts from three levels, as the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero.

Mostly cascaded multilevel inverter is used due to its ease of design. H bridge type of multilevel was later used. Then clamped type of inverter was implemented. In the clamped type inverter the clamping is done by diode, capacitor and by neutral clamping method.

The main objective of multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, which are typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion[20].

![Figure 1 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels](image)

In Figure 1(a) the output Va can take values i.e. 0 and Vc as possible values. In Figure 1(b) the output Va can take three possible values i.e. 0,Vc and 2Vc. In Figure 1(c) the output Va can take four possible values i.e. 0, 0.5Vc, 2Vc and 3Vc. It can be extended further. The number of possible outputs presents the level of the inverter that is shown in figure 2.

1.1 Neutral point clamped inverter (NPC)

The neutral point clamped topology is also known as diode clamped topology. The main advantage of the NPC topology is that it
The authors in [18] proposed a novel high efficiency. The three-level IFFC system for low leakage current and dead time elimination. Based on the foregoing recognitions, the T-type 3L-NPC, as shown in Figure 4, is being studied increasingly to improve the system efficiency. The authors in [10] evaluated the power loss and control scheme of T-type 3L-NPC applied in the low-voltage renewable energy system. The authors in [11] applied T-type 3L-NPC in a solar system to avoid the high conduction loss.

3 PROPOSED DIODE FREE T-TYPE 5L-NPC INVERTER AND ITS PWM STRATEGY

- The proposed diode free T-type 5L-NPC inverter for low-voltage renewable energy systems is shown in Figure In this new topology, two 600-V CoolMosfets in the reverse serial connection, replaces the IGBT + diode bidirectional middle switch in the conventional T-type 5L-NPC.

- Thus, in this topology, four CoolMosfets form a parallel current path to reduce the equivalent ON-state resistance. More importantly, the zero-vector current flows through two CoolMosfets in the reverse connection; hence, no body diode is involved in the current path even with the non-unity power factor.

The circuit design of proposed system is shown in the Figure 7. In this a low voltage DC source is connected to the inverter supply side. A cumulative pair of four switches is placed in t-type inverter topology. The middle point of the cool MOSFET switch pair N can be defined as the neutral point. The staircase voltage synthesis can be explained as, the neutral point n is considered as the output phase.
voltage reference point four complementary switch pairs exist in each phase. By turning on one of the switches will exclude the other from being turned on this type of switch is called as complementary pair switch. The diode free neutral point clamping becomes the most convenient way for designing high-voltage high-power applications without the clamping diode.

The PWM strategy for the new topology is shown in Figure 6. With the new PWM strategy, the corresponding topological states is with the unity power factor. The current commutation within the reactive power generation region is shown in Figure 6. Here six pulses are generated for the switching the cool MOSFET in the 5l-NPC.

The figure 8 shows the five level inverter output. The MOSFET switches the voltage level step by step to attain five level waveform with reduced harmonic distortion (THD=0.346). From the figure 8, it is clear that the output is continuous in the succeeding cycles. On increasing the levels the THD of the system will be reduced.

<table>
<thead>
<tr>
<th>Type</th>
<th>Comment</th>
<th>Part number</th>
<th>Quantity</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional T</td>
<td>IGBT</td>
<td>IKW40N120H3</td>
<td>2</td>
<td>3.1$</td>
</tr>
<tr>
<td></td>
<td>IGBT+Diode</td>
<td>FGH40N60</td>
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<td>1.6$</td>
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<td>Conventional T with Mosfet</td>
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<td>IKW40N120H3</td>
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<td>3.1$</td>
</tr>
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<tr>
<td>Novel T with Coolmos</td>
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<td>CoolMos</td>
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<td>4</td>
<td>3.8$</td>
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</tbody>
</table>

The above table defines the cost of devices used for both T type and for T type inverter. On reducing the number of switches the cost of system will be reduced. In the proposed system the 5-level NPC inverter consists of one bidirectional and four switches.

In this contra flow current is totally negotiated by Mosfet. So that the system do not suffer from component stress, the cost of the system is tolerable when compared with 3l-NPC. Hence the I–type of system will cost high so the T-type is preferred.
The total harmonic distortion of 5-level NPC inverter with diode is defined in the below figure 8. The THD of 5-l NPC with the cool Mosfets is shown in figure it define that the harmonic loss due to long conduction is reduced and the THD is also reduced to a tolerable level.

The system with cool Mosfet switch provide limited conduction path, due to elimination of diode in the conduction path results in short conduction path with zero vector clamping voltage. The THD waveform of diode free T-type 5l-NPC inverter is shown in figure 10.

5 CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. Multi-level PWM inverters, (including five-level inverters) have significant operational advantage, such as the ability to drive a motor with nearly sinusoidal current waveforms and at higher output voltages. The multilevel inverter topology can overcome some of the limitations of the conventional three-level inverter. Output voltage and power increase with number of levels. Harmonics decreases as the number of levels increase. In addition, increasing output voltage does not require an increase in voltage rating of individual force commutated devices. Recently, active schemes of inverter topologies and PWM strategies have been introduced in several literatures for both two-level and multi-level inverters to reduce or even eliminate common-mode voltage.

There are many multilevel inverters developed according to the voltage levels required. This project deals with the design and implementation of single-phase five-level neutral point clamped inverter. The sinusoidal PWM technique is involved in the design which has several advantages over other modulation techniques. The operational and the switching functions are analyzed in detail. In addition it is compared with the conventional three-level PWM inverter, smaller filter size, improved output waveform and other advantages.

The simulation results shows that the developed five-level PWM inverter has many merits such as

- Lower EMI,
- Less Harmonic Distortion.
- Improves the power quality and dynamic stability for utility systems.

The THD of the proposed inverter is considerably alleviated and the dynamic responses are also improved significantly.

REFERENCES


**AUTHOR’S PROFILE**

Krishna KC obtained his B.E. in Electrical and Electronics Engineering,(VEL TECH ENGINEERING COLLEGE,2013), M.E. in Applied Electronics (HINDUSTHAN COLLEGE OF ENGG & TECHNOLOGY, 2015).He is currently doing his project work on Diode Free T-Type Five Level Neutral Point Clamped Inverter for Low Voltage DC System.

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