Design And Implementation Of Low Power Approximate Multiplier

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Abstract: Multiplier is one of the arithmetic operations that are used in VLSI circuits. In this paper, the approximate multiplier is designed. Approximate multiplier is designed by using MUX with OR logic. Approximate multiplier will reduce the transistor count, power consumption, delay and it provides high speed output compared to Array multiplier. Removing of error is not necessary for certain application such as, image processing and video processing. Area and speed in approximate multiplier is efficient than the conventional multipliers. In this adder mainly used in DSP Application, Image Processing. The result of approximate multiplier is compared to the array multiplier. The simulation result shows the low power consumption by using Xilinx ISE simulation tool.

Key words: Approximate multiplier, OR gate, MUX logic, Low power consumption, Array Multiplier.

INTRODUCTION

Generally in VLSI design, the result will always be definite and accurate. The adder and multiplier are an important role in the design. In much application the analog signal is given as input and the analog signal is converted into digital signal by using sampling method. The noisy channel has already occurred in the digital signal before converting to the analog signal\cite{8}. Due to overcome these problems, IC’s designed has improved in transistor size scaling. If the circuit contains any internal and external errors or imperfect result, hence, it is consider as error tolerant circuit. This problem is solved by using adders and multiplier. Even though using adders and multipliers, it does not produce well performance result in speed, power consumption, delay and area. The error tolerant concept is not required in all digital system, it only required in control system\cite{9}. In proposed system approximate adder is used and it gives much better result when compared to the conventional adders.

EXISTING SYSTEM

The full adders are used in multiplier for simplifying the multiplication. In existing system, they use Static Energy Recovery Full (SERF) adder. This adder consists of 10 transistors. The gate of transistors are controlled by the input signal of full adder. SERF adder does not have any direct connection to the ground. So, the design become a short circuit due to power dissipation is reduced completely\cite{5}. This is a way for recover the static energy. The applied voltage should be reused by charging of load capacitance. SERF adder does not use any inverting input. And, This adder is well performed in higher voltage. But, the supply voltage is lesser than 0.3V then the design is fail to work. The main advantage of SERF adder does not need any inverting input.
The output equation of SE\textsuperscript{RF} adder is,
\[ \text{Sum} = (A(XNOR)B)Cin + (A(XOR)B)Cin \]
\[ \text{Cout} = (A(XOR)B)Cin + (A(XNOR)B)A \]

When applying \( A=1, B=1 \) and \( Cin=0 \), the output signal reach only 0.1V. It is not enough to change the state of the next stage.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Cin</th>
<th>Sum</th>
<th>Cout</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Vdd-Vth</td>
<td>( \approx 0 )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>( V_{tp} )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Power consuming</td>
<td>Vdd-2Vth</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( \text{&gt;Vdd-2Vth} )</td>
<td>( Vdd-Vth )</td>
</tr>
</tbody>
</table>

Truth table of SE\textsuperscript{RF} adder

SERF adder includes another problem, such as F node is connected to 0. When applying Cin is equal to one (Cin=1), Cout is charged to Vdd. And applying Cin is equal to one (Cin=0) Cout must be discharge using PMOS transistor, and it is not fully discharged\[5\]. In this case, two PMOS transistors, and one NMOS transistor is on. And the output is dependent upon the transistors.

By applying low voltage the SERF adder involves serious problems.

![SERF Adder](image)

The below diagram is a part of SERF adder, it explained a case of \( A \& B = 0, Cin = 0 \) in the adder.

![Equivalent circuit of ‘110’](image)

**ARRAY MULTIPLIER**

In digital signal processing, multipliers are play an important role for multiplication. Array multiplier performs add and shift operations by using add & shift algorithm\[5\]. The main component of multiplier is multiplicand and partial product.
The partial products are produced by multiplying each bit of the two inputs. And the partial products are shifted and carry is added to next stage.

Array multiplier is performs the signed multiplication. In order to equal length of the inputs are multiplied and produce same length of the output. Multiplier architecture is divided into three stages, Partial product generation, Partial product reduction and the final addition of the reduced. The speed of multiplier can be improved by reducing the number of partial products.

Fig. 4 bit multiplication

PROPOSED SYSTEM

To overcome the problem of SERF adder, we introduce the approximate multiplier. The approximate multiplier consists of seven logics. It reduces the area, delay and power consumption compared to array multiplier. To achieve the parallel process of data in adder by cutting the carry propagation chain[6]. The approximate multiplier is suitable for image processing and it result is similar to accurate multiplier. The carry signal only propagates one bit higher in any situation in this approximate adder. A simple tree of the approximate adders is used for partial product accumulation and the error signals are used to compensate the error for obtaining a better accuracy[7].

The Approximate multiplier is used to multiply two eight bits. And, produce a sixteen bit output. The eight bit inputs are divided into two segments. Each segment has consists of four bits.
The approximate multiplier consists of three mux, two OR gate, and one half adder. Mux is used to select the one output from the many inputs. The selection process is done by the selecting inputs from the OR gate.

![Approximate Multiplier](image)

**SIMULATION RESULT**

The simulation result shows the power consumption of approximate multiplier. The table shows the power requirements of proposed multiplier such as dynamic, quiescent and total power consumption.

Table. Power consumption of approximate multiplier.

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Dynamic Power (mW)</th>
<th>Quiescent Power (mW)</th>
<th>Total Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2569</td>
<td>1312</td>
<td>32</td>
<td>1344</td>
</tr>
<tr>
<td>2</td>
<td>2070</td>
<td>1089</td>
<td>32</td>
<td>1121</td>
</tr>
<tr>
<td>3</td>
<td>480</td>
<td>74</td>
<td>128</td>
<td>102</td>
</tr>
<tr>
<td>4</td>
<td>6770</td>
<td>38</td>
<td>148</td>
<td>186</td>
</tr>
</tbody>
</table>

The proposed multiplier is produces an approximate result. Some time it produce exact result of a given input.
CONCLUSION

In this paper, we proposed the design and simulation of an 8-bit approximate multiplier. The total number of transistors used in approximate multiplier is reduced to seven logics. It is easy to say the area and delay of approximate multiplier is reduced than the array multiplier. And, the total power consumption of Approximate multiplier is 0.883W. And, it is used for signal and image processing.

REFERENCE


