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Design of an ADC using High Precision Comparator with Time Domain Offset Cancellation

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Abstract— The comparator is a combinational logic circuit that plays an important role in the design of analog to digital converter. One of its most important properties is its input referred offset. When mismatches are present in a dynamic comparator, due to internal positive feedback and transient response, it is always challenging to analytically predict the input-referred random offset voltages since the operating points of transistors are time varying. To overcome the offset effect a novel time-domain bulk-tuned offset cancellation method is applied to a low power dynamic comparator. Using this comparator in analog to digital converter it does not increase the power consumption, but at the same time the delay is reduced and the speed is increased. The comparator is designed using the 250-nm CMOS technology in mentor graphics tool. Operating at a supply voltage of 5v and clock frequency 100MHZ, the comparator together with the offset cancellation circuitry dissipates 335.49nW of power and dissipates 1.027uW of power for comparator without offset cancellation circuit. The simulation result indicates that the offset cancellation circuitry consumes negligible power and it does not draw any static current. Using this high precision offset cancelled comparator in the analog to digital converter circuit the static power consumption is less and it is able to work under very low supply voltage.

Index Terms— Offset Cancellation (OC), Signal to Noise Ratio (SNR), Output Offset Storage (OOS), Phase Detector (PD), Charge Pump (CP).
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1 INTRODUCTION

A NALOG-TO-DIGITAL converters (ADCs) are very important building blocks in modern signal processing and communication systems. For signal processing, digital domain is preferred over analog domain because of its advantages such as noise immunity, storage capability, security etc. For long distance, digital communication is more reliable due to regenerative repeater. Due to these, today nearly all modern electronics are primarily digitally operated, allowing for advanced digital signal processing (DSP). But the real world signals such as signals coming from various transducers are analog in nature. This analog signal must be converted into digital to allow digital signal processing. Similarly after signal processing in digital domain, the signal is converted back into analog. The applications of ADC include DC instruments, process control, thermocouple sensors, modems, digital radio, video signal acquisition etc.

2 OFFSET CANCELLATION COMPARATOR

In a low-power comparator using the offset cancellation (OC) scheme, it is able to sense the offset in the time domain and eliminate it in closed loop by tuning the body voltages of the input transistors. It can achieve arbitrarily fine resolution and exponential convergence of the residual offset, so that the trade-off between resolution, convergence speed and initial offset range is avoided. In addition, the OC circuitry only requires a single phase clock to operate and adds negligible power and delay to the comparator.

The two-stage dynamic comparator core used in this design is inspired by the double-tail voltage sense amplifier. Firstly, the second stage is asynchronously clocked by the outputs of the first stage. This eliminates the need for a complementary clock, and improves resolution by input dependent positive feedback.

The proposed OC scheme senses the comparator offset by measuring the delay between the two

outputs and cancels it by tuning the body voltages of the input transistors. In the ideal case in which all the transistors are matched, if the two inputs of the comparator are equal, Vo+ and Vo- will fall simultaneously at an identical rate at the falling edge of clock, whereas in the presence of offset, they will not. Therefore, the input-referred offset can be represented by the delay between the two complementary outputs when there is no differential input. A phase detector (PD) detects the polarity and magnitude of this delay and drives a charge pump (CP). The CP changes the body voltages of the comparator input transistors stored in the capacitors Cb+ and Cb-.

The body voltage affects the threshold as given in the (1) as

$$|V_{tp}| = |V_{t0}| + \gamma\left(\sqrt{|V_{SB}| + 2\varphi_F} - \sqrt{2\varphi_F}\right) \quad (1)$$

where Vtp is the threshold of the input transistor, Vt0 is the threshold with zero body bias, and γ, Φ_f are process dependent parameters.

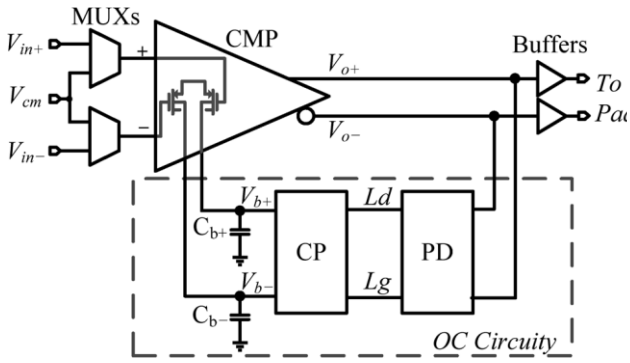

Fig. 1. Comparator offset cancellation

A multiplexer or MUX is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. The function of the PD is to sense the delay between its two inputs. A phase detector is a logic circuit that generates a voltage signal which represents the difference in phase between two input signals.

3 ADC WITH OFFSET CANCELLATION COMPARATOR

The analog to digital converter can be designed using the offset cancelled comparator to work under low power consumption. Using this scheme in ADC it does not increase the power consumption, but at the same time the delay is reduced and the speed is increased.

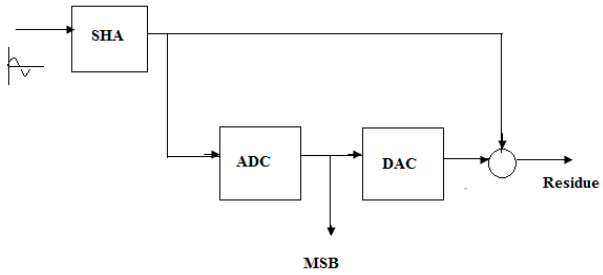

Fig. 2. The block diagram of the system

To achieve a high conversion speed, the simplest and potentially the fastest, flash architecture is used in this architecture. In a flash architecture, clocked comparators offer polarity sampling as one of the advantage to the circuit. Consequently, the comparator outputs constitute a thermometer code, which is converted to binary by the decoder. Comparators often incorporate clocked regenerative amplifiers to achieve a high speed. In this ADC architecture the design flows through the following steps.

1. First, the input signal is captured by the sample and hold amplifier.
2. Second, this signal is quantized by the sub-ADC, which produces a digital output.
3. Third, this digital signal goes to the sub-DAC which converts it to an analog signal. This analog signal is subtracted from the original sampled signal - thereby, leaving a residual signal.
4. Fourth, this residual signal is increased to the full scale through the inter-stage amplifier.

4 IMPLEMENTATION

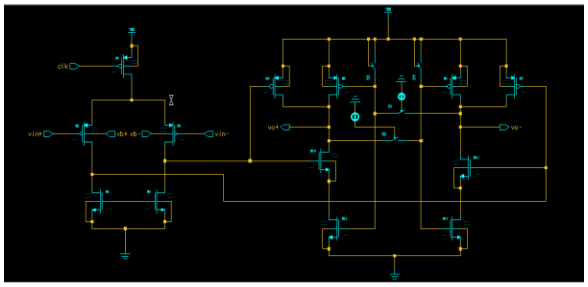

Fig. 3. Design of two stage comparatorcircuit with the offset cancellation circuitry. In this the switches s1 and s2 are open and the switches s3 and s4 are kept closed.

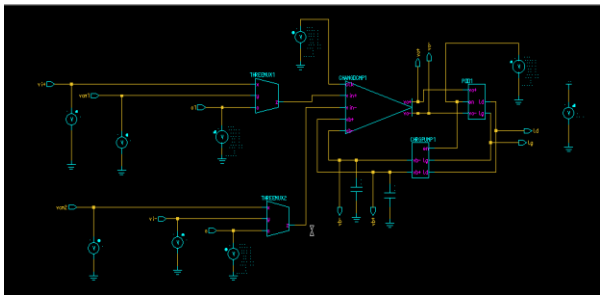

Fig. 4. Design of an offset cancelled comparatorwith time domain bulk-tuned offset cancellation. In this the MUX selects the input signals for different operation modes. The comparator compares the two input signal and generates the corresponding output signal. The phase detector senses the delay from the comparator outputs and drives a charge pump. The charge pump changes the body voltages of the input pair stored in Cb+ and Cb-, and cancels the offset.

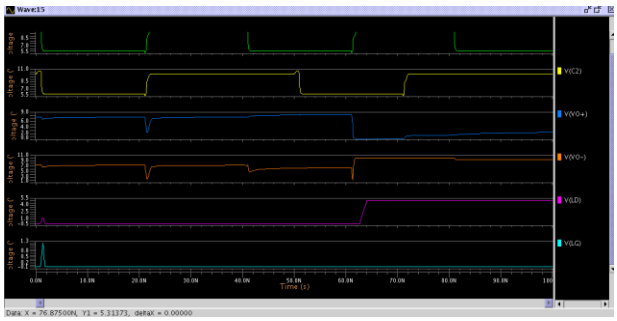

Fig. 5. Outputwaveform of the comparator with offset cancellation circuitry. In this due to the offset, the falling edge of Vo+ leads the Vo-. So that the phase detector senses this delay and generates pulses on lead signal pin. Similarly the lag signal is generated when Vo+ lags Vo-.

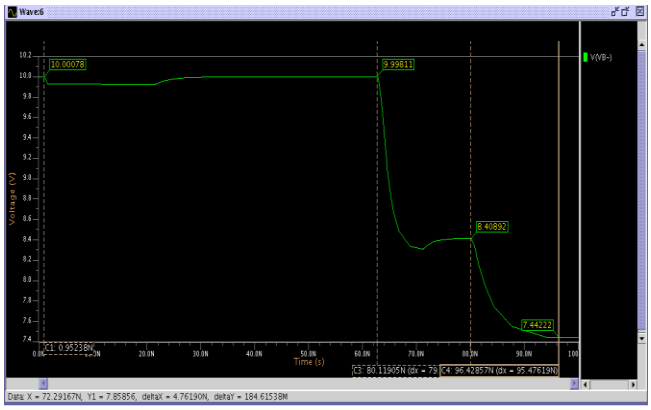

Fig. 6. The output waveform of the comparator body voltage calculation. If Vo+ leads Vo-, then Vb- will be decreased by while the other remains constant.

This signal reduces the offset generated by the various transistors in the circuit. The body voltage difference ΔVb is calculated from this figure

. The body voltage difference is calculated as

$\Delta Vb = (Vb-) - (Vb+)$

$= 9.999 - 7.442$

$= 2.55$ V

TABLE 1
COMPARISON OF WITH AND WITHOUT OC COMPARATOR

S.No	Parameters	Without OC	With OC
1.	Power Dissipation	335.49 nw	1.0275 uw
2.	Input referred offset	5.415 mV	50.57 uV
3.	Body voltage difference	0V	2.55V

5 CONCLUSION

The result showed that the power consumption of a comparator with offset cancellation circuit consumes less power than the comparator without offset cancellation, and at the same timethedelayisreducedand the speed is increased. The OC circuit circuitry does not draw any static current and this proposed scheme can be repeated frequently without consuming excessive time or power. By calculating the body voltage difference from the lead, lag signal the offset is cancelled in the output signal. As the number of iterations increases the

offset can be proportionally reduced. It is worth noting that both the proposed comparator and OC scheme are very amenable to process scaling because of their dynamic and time-domain operation. While the accuracy of the circuit will be degraded due to the reduced drain resistance, the proposed scheme will actually benefit from smaller feature size because it can provide smaller parasitic capacitance and higher time resolution. The design is also tolerant to supply scaling because there is no stacking of transistors.

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