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PV Based High Level Hybrid Multilevel Inverter Using Field Programmable Gate Array

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Abstract— This paper presents a PV based high level hybrid multilevel inverter using field programmable gate array. Sepic converter is the developed converter derived from the buck-boost converter. In this proposed model the Sepic-converter eliminate the output ripples and effectively enhance the output voltage level. Cascaded H Bridge & Neutral point clamped (NPC) inverter topologies are hybridized to obtain 127 level of output voltage using reduced number of switches and DC sources. By increasing the number of voltage level, the Total Harmonic Distortion (THD) can be reduced and hence reduction in size of the filter. MATLAB simulation is carried out to verify the performance of the proposed system.

Index Terms— Sepic converter, Hybrid multilevel inverter, Cascaded H bridge & NPC inverters, Total Harmonic Distortion.

1 INTRODUCTION

THE limitation of conventional energy sources and environmental issues such as global warming and pollution is prompting the world toward the development of renewable energy sources. Photovoltaic (PV) plays an important role in power production among more traditional energy sources such as oil, coal, nuclear, hydro and wind [1]. PV array may directly feed small loads such as lighting systems and DC motors. More sophisticated applications require electronic converters to process the electricity from the array. These converters may be used to regulate the voltage and current at the load, to control the power flow in grid-connected systems and mainly to track the maximum power point (MPP) of the array. Converters with the maximum power point tracking (MPPT) feature use an algorithm to continuously detect the maximum instantaneous power of the PV array. Because the operating conditions of the array (solar irradiation and temperature) may change randomly during the operation of the system an MPPT algorithm is necessary so that the maximum instantaneous power can be extracted and delivered to the load.

Over the few past decades, different MPPT techniques are implemented and proposed [2] to track the maximum power from the PV system. The methods vary in complexity, sensors required, convergence speed, cost, range of effectiveness, implementation hardware, popularity, and in other respects. The simplest MPPT technique analyzed in [2], [3] and [4] is the perturb and observe (P&O) method.DC voltage obtained from the PV panel contains high voltage ripples and it is not constant. DC-DC converters are employed to attenuate the ripples regardless of change in load voltage. The conventional converter does not meet the load requirement containing more ripples on the output voltage and parasitic effects. To overcome this problem the advanced developed DC-DC Sepic converter technology was introduced [5].

Sepic converter is the developed converter derived from the buck-boost converter, which performs buck or boost operation [6], [7]. Sepic converters have the characteristics of high voltage transfer gain, high power density, and reduced ripple in voltage and current in simple topology. In this proposed converter the additional filter elements can be used to eliminate the output ripples and effectively enhance the output voltage level. It overcomes the parasitic problems present in the classical dc-dc converter.The various inverter topologies for interfacing photovoltaic modules to the grid is presented in [8], which involves two major tasks. One is to inject a sinusoidal current into the grid and another one is to check the PV module(s) is operated at the MPP, which is the operating condition where the most energy is captured. This is carried out by using MPP tracker. In order to achieve a utilization ratio of 98% the amplitude of the ripple voltage should be below 8.5% [8]. To interface the PV module(s) with the grid the inverter topologies must follow some standards. In recent day's Multi level inverter (MLI) technologies has achieved its wide acceptance in the area of high power medium voltage energy control. It includes an array of power semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms. In comparison with a two-level voltage source inverter (VSI), the multilevel VSI can produce more number of levels in the output voltage [9]. Hence, by increasing the number of levels in the MLI, the output voltage has more steps in generating a staircase waveform, which has a reduced total harmonic distortion (THD). The Diode clamped, Flying capacitor, Cascaded H-bridge inverter are the three main multilevel inverter structures which are used in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter. But in the cascaded H-bridge inverter, separate dc sources are needed for each H-bridge. It will result in higher number of dc input sources [10]-[12]. In order to improve power quality and reduce EMI problems, it is required to increase the number of levels [13]. The number of switches becomes too high with higher number of voltage levels if all the DC busses are at same voltage; this also increases the number of gate drivers and higher conduction loss of devices. All above factor will have negative impact on cost, reliability (reliability is inversely proportional to

number of components) and efficiency. The asymmetric structure of multilevel inverter can increase the number of levels without dramatic increase in number of switches [14]. So, to overcome the above mentioned problems the two multilevel inverter topologies are mixed to obtain higher number of output voltage level by using lesser number of switches and sources [15], [16]. In this proposed system the Cascaded H-Bridge & Neutral Point Clamp topologies are hybridized to form this topology. Increasing the number of voltage levels gives more flexibility to reduce Total Harmonic Distortion (THD) of the system and in turn reduction in cost and size of the power filter.

2. PROPOSED TOPOLOGY DESCRIPTION

In this proposed system the photovoltaic is used as a DC source. The DC-DC Sepic converter provides constant DC supply and also used to eliminate or reduce the output voltage and current ripples. Here, to get a maximum power from the panel, to generate a switching pulse for the converter switches the MPPT with control unit is used. A typical solar panel converts only 30 to 40 percent of the incident solar irradiation into electrical energy. In order to continuously harvest maximum power from the solar panels, they have to operate at their maximum power point (MPP). This is why the controllers of all solar power electronic converters employ some method for maximum power point tracking (MPPT). There was a different MPPT techniques [1] are available.

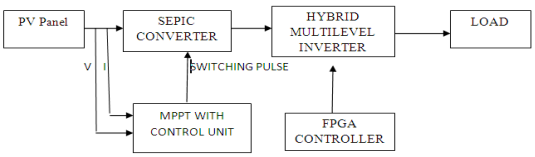


Fig. 1. Block diagram of proposed system

Among various types of techniques Perturb & Observe (P&O) is proposed in this system. It's the simplest and most commonly used method. In this method, the sign of the last perturbation and the sign of the last increment in the power are used to decide what the next perturbation should be. If there is an increment in the power, the perturbation should be kept in the same direction and if the power decreases, then the next perturbation should be in the opposite direction. Based on these facts, the algorithm is implemented. The process is repeated until the MPP is reached [4].

A. Converter circuit operation

The DC-DC conversion technology is a major subject area in the field of power electronics and drives. These converters are widely used in industrial applications and computer hardware circuits. The proposed DC-DC sepic converter topology provides stable and ripple free output voltage and current [8]. DC voltage obtained from the PV panel contains high voltage ripples and it is not constant. The conventional converter does not meet the load requirement containing more ripples on the output voltage and parasitic effects.

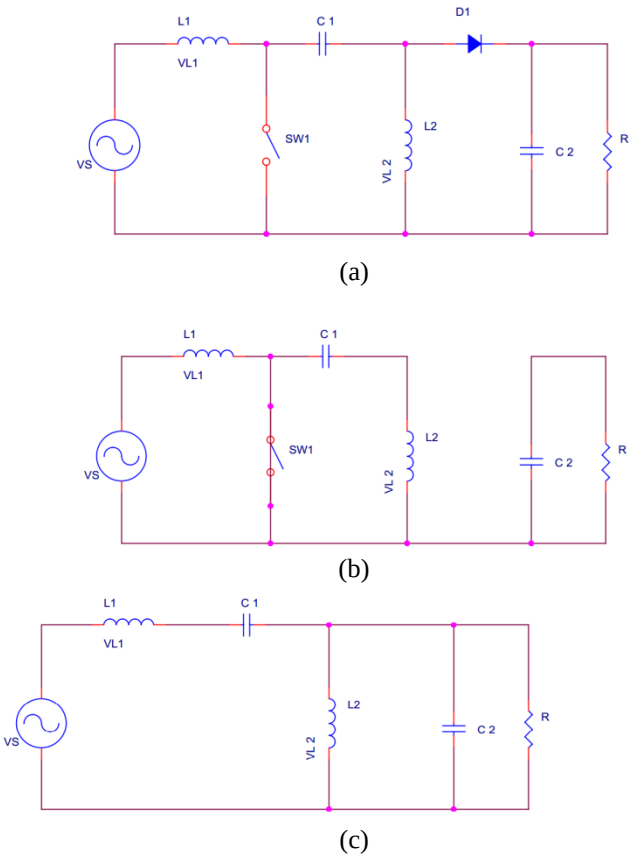


Fig. 2. SEPIC converter circuit operations

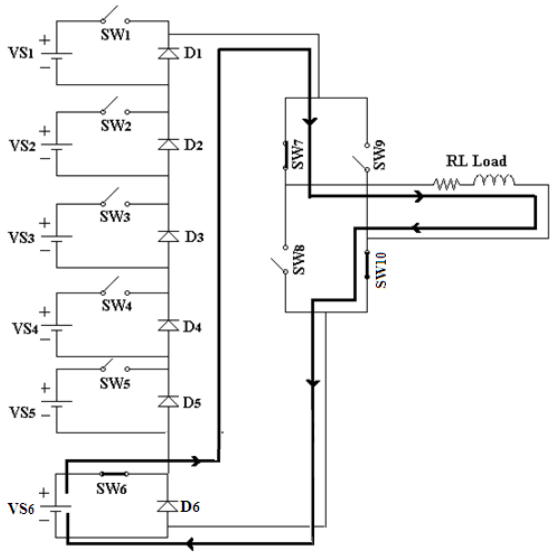
In Fig. 2(b) when the switch is ON the inductor L1and L2 gets charging in reverse flow, in that time there is no output across the load R. In Fig. 2(c) when the switch is in OFF position the same current of L1.the L2 will continuous in negative direction. However is being charged by L1 during this OFF cycle and will in turn recharge L2 during the ON cycle.

B. Inverter circuit operations

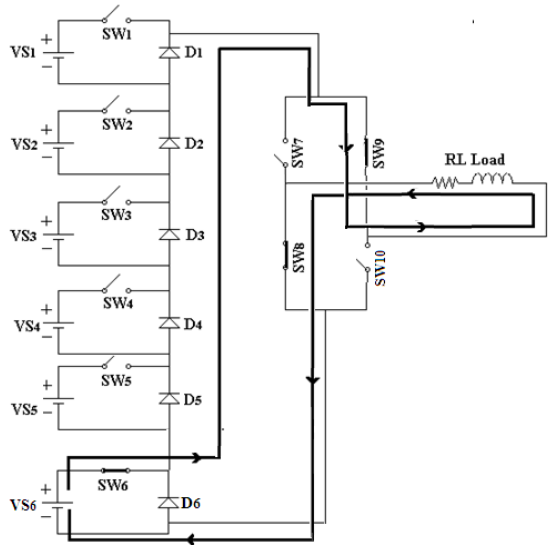
Though multilevel inverter has a number of advantages it has drawbacks in the vein of higher levels because of using more number of semiconductor switches and isolated dc sources. This may leads to vast size and price of the inverter is very high. In order to overcome this problem the new multilevel inverter topology is proposed with reduced number of switches and sources. As a result it is possible to reduce or even to eliminate output filters. The unified analysis and design consideration for hybrid multilevel inverter has been proposed in [15]. In this proposed system the Cascaded H-Bridge & Neutral Point Clamp topologies are hybridized.

In fig. 3(a) when the switch SW6 is turned ON the current flow will be in the direction of VS_6 (+) – SW_6-D_5- D_4- D_3- D_2- D_1- SW_7- RL Load (+)- RL Load (-)- SW_{10}- VS_6 (-). During this time the diode D6 will not conduct. The output voltage and current will be positive. The switches in the H bridge SW_7 and SW_{10} are turned ON for the operation of inverter in the positive half cycle. The inverter operation

for the first level in negative cycle is shown in fig.3 (b), when the switch SW_5 is turned ON the current flow will be in the direction of VS_5 (+)-SW_5-D_4-D_3-D_2-D_1-SW_8-RL Load (-)-RL Load (+)-SW_7-VS_5 (-). The output voltage and current will be negative. The switches SW_8 and SW_9 in the H Bridge are turned ON for the operation of inverter in the negative half cycle.



(A)



(B)

Fig. 3. (a) Inverter operation for the first level in positive cycle
(b) Inverter operation for the first level in negative cycle

. Similarly the remaining level is obtained by alternatively ON and OFF of the switches as per the switching states given in the following table. The switching state is given for the 63 level of positive half cycle only. It will be same for the negative cycle but the difference is, when the switches SW_7 and SW_{10} are conducting the inverter output voltage and current will be in positive half cycle, when the switches SW_8 and SW_9 are conducting the inverter output voltage and current will be in the negative half cycle.

TABLE 1 SWITCHING STATES

Level	Neutral point clamped inverter(NPC)						Cascaded H-bridge inverter(CHB)			
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
1	0	0	0	0	0	1	1	0	0	1
2	0	0	0	0	0	0	1	0	0	1
3	0	0	0	0	1	1	1	0	0	1
4	0	0	0	1	0	0	1	0	0	1
5	0	0	0	1	0	1	1	0	0	1
6	0	0	0	1	1	0	1	0	0	1
7	0	0	0	1	1	1	1	0	0	1
8	0	0	1	0	0	0	1	0	0	1
9	0	0	1	0	0	1	1	0	0	1
10	0	0	1	0	1	0	1	0	0	1
11	0	0	1	0	1	1	1	0	0	1
12	0	0	1	1	0	0	1	0	0	1
13	0	0	1	1	0	1	1	0	0	1
14	0	0	1	1	1	0	1	0	0	1
15	0	0	0	1	1	1	1	0	0	1
16	0	1	0	0	0	0	1	0	0	1
17	0	1	0	0	0	1	1	0	0	1
18	0	1	0	0	1	0	1	0	0	1
19	0	1	0	0	1	1	1	0	0	1
20	0	1	0	1	0	0	1	0	0	1
21	0	1	0	1	0	1	1	0	0	1
22	0	1	1	1	1	0	1	0	0	1
23	0	1	1	1	1	1	1	0	0	1
24	0	1	1	0	0	0	1	0	0	1
25	0	1	1	0	0	1	1	0	0	1
26	0	1	1	0	1	0	1	0	0	1
27	0	1	1	0	1	1	1	0	0	1
28	0	1	1	1	0	0	1	0	0	1
29	0	1	0	1	0	1	1	0	0	1
30	0	1	0	1	1	0	1	0	0	1
31	0	1	0	1	1	1	1	0	0	1
32	1	0	0	0	0	0	1	0	0	1
33	1	0	0	0	0	1	1	0	0	1
34	1	0	0	0	1	0	1	0	0	1

35	1	0	0	0	1	1	1	0	0	1
36	1	0	1	1	0	0	1	0	0	1
37	1	0	1	1	0	1	1	0	0	1
38	1	0	1	1	1	0	1	0	0	1
39	1	0	1	1	1	1	1	0	0	1
40	1	0	1	0	0	0	1	0	0	1
41	1	0	1	0	0	1	1	0	0	1
42	1	0	1	0	1	0	1	0	0	1
43	1	0	0	0	1	1	1	0	0	1
44	1	0	0	1	0	0	1	0	0	1
45	1	0	0	1	0	1	1	0	0	1
46	1	0	0	1	1	0	1	0	0	1
47	1	1	0	1	1	1	1	0	0	1
48	1	1	0	0	0	0	1	0	0	1
49	1	1	0	0	0	1	1	0	0	1
50	1	1	1	0	1	0	1	0	0	1
51	1	1	1	0	1	1	1	0	0	1
52	1	1	1	1	0	0	1	0	0	1
53	1	1	1	1	0	1	1	0	0	1
55	1	1	1	1	1	0	1	0	0	1
55	1	1	1	1	1	1	1	0	0	1
56	1	1	1	0	0	0	1	0	0	1
57	1	1	0	0	0	1	1	0	0	1
58	1	1	0	0	1	0	1	0	0	1
59	1	1	0	0	1	1	1	0	0	1
60	1	1	0	1	0	0	1	0	0	1
61	1	1	0	1	0	1	1	0	0	1
62	1	1	0	1	1	0	1	0	0	1
63	1	1	0	1	1	1	1	0	0	1

The parameter and its values which is used in simulation is given below.

S. No	Parameters	Values used in simulation
1	DC input voltage	19.1 V
2	Inverter output voltage	230 V
3	Total number of switches	11
4	Inductance (L1, L2)	45µH, 1.5mH
5	Capacitance (C1, C2)	20µF, 100µF
6	Number of level	127

In this proposed system the sepic converter boost up the input DC voltage to 230V and it can be splitted into six input sources for the inverter switches by using multiple output DC/DC converter. The ripples in the output can be eliminated by using filter elements (L2 & C2). By alternatively turning ON and OFF of the inverter switches (SW_1-SW_6) the 127 level of output voltage is obtained and it is converter into AC by means of CHB switches (SW_6-SW_8) which perform the operation of conventional inverter.

3. SIMULATION RESULTS

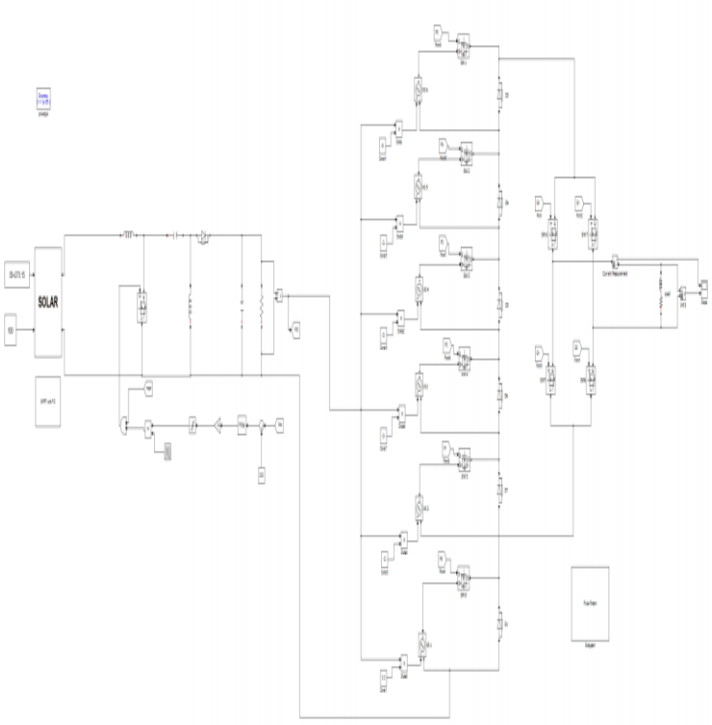


Fig 4. Simulation circuit for proposed system

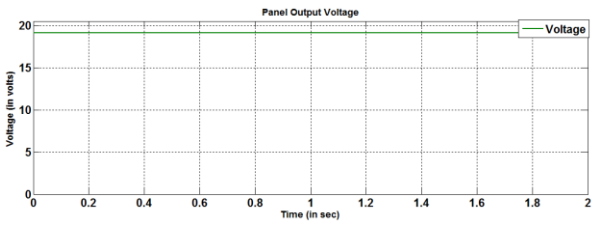


Fig. 5 (a) PV panel output voltage

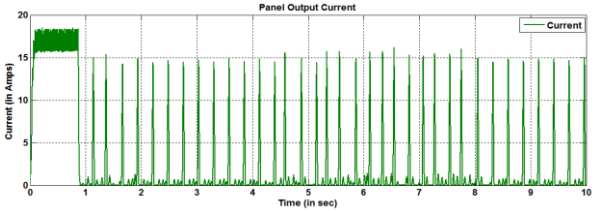


Fig. 5. (b) PV panel output current

The fig 5(a) shows the output voltage waveform for solar panel. The voltage magnitude is about 19.1 V. This voltage is not constant enough. To converter this voltage into constant DC this will be send into DC-DC sepic converter. The fig 5(b) shows the output current waveform for solar panel. The current magnitude is around 15 A.

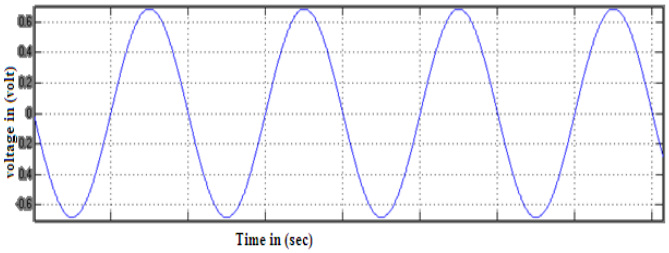


Fig 6. (a) Inverter output127 level

The fig 6(a) shows the output voltage waveform for proposed Hybrid multi level inverter. The output voltage having 127 level. Hence THD can be reduced by using proposed inverter topology.

4. CONCLUSION

This paper presents a PV based hybrid multilevel inverter using field programmable gate array. In this proposed DC-DC sepic converter the additional filter elements eliminate the output ripples and effectively enhance the output voltage level. It overcomes the parasitic problems present in the classical dc-dc converter. The 127 level of output voltage is obtained by using proposed Hybrid multilevel inverter topology. Hence the THD is reduced. The presented concepts have been verified in simulations and validated experimentally.

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