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High Speed Carry Skip Logic by Using Concatenation and Incrementation Scheme

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Abstract—In our paper, we proposing a high speed and energy efficient carry skip adder known as concatenation and incrementation carry skip adder(CI-CSKA).In this we are adding an incrementation block in addition to the conventional structure of carry skip adder and replaces the multiplexer logic with low power gates such as AOI and OAI gates for performing skip operation .The drawback of this modified structure is the increased power consumption while it can be used in high speed application .This difficulty is overcome by replacing some of the RCA block in the modified structure with binary excess converter .This method reduces power consumption by maintaining the speed. Xilinx ISE 8.1i software is used to verify the simulation result and Modelsim is used to obtain waveform representation of the model.

Index Terms --CSKA, CI-CSKA, BEC, OAI, AOI, CSLA

1. INTRODUCTION

Adders are the basic building block of arithmetic and logic units (ALUs) [1] and majority of digital signal processing (DSP) application the critical operation are the addition, multiplication and accumulation. Addition is an important operation for any digital system .Hence increasing their speed and reducing their power/energy consumption strongly affects the speed and power consumption of processors. Many different adder architecture for speeding up binary addition have been studied and proposed over the last decades .There are many works on the subject of optimizing the speed and power of these units, which have been reported in [2].Efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design .One of the technique is to reduce the power consumption is the reduction of supply voltage. In addition to that different adder architecture are discovered with different delay, power consumption and area usages.

Examples include ripple carry adder (RCA),Manchester carry chain ,carry skip adder (CSKA),carry look-ahead adder, carry select adder (CSLA),conditional sum ,and various parallel prefix adder are available to satisfy different area, delay and power requirements. The RCA has the simplest layout with smallest area and power consumption but critical path delay is high. In the CSLA, the speed is higher but the power consumption, and area usages are considerably larger than that of the RCA. The PPAs, which is the high speed adder that uses propagate and generate scheme for performing addition. There are different types of the parallel prefix adders that lead to different PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) is one of the fastest structures but results in large power consumption and area usage.

The structure complexities of PPAs are more than those of other adder schemes.In this paper given the attractive features of carry skip adder structure, which is an efficient adder in terms of area and the power consumption. Comparatively lower speed of this adder limits its use for high speed applications .We have focused on reducing its delay by modifying its structure. The speed enhancement is achieved by concatenation and incrementation method, also here replaces the multiplexer logic which is used to perform the skip operation in conventional carry skip adder with the low power gates such as and-or- invert(AOI) and or-and-invert(OAI).Thus the modified structure is known as concatenation and incrementation adder(CI-CSKA).

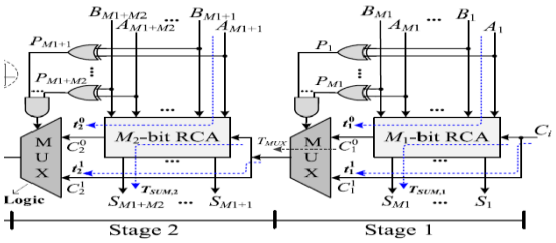


Fig. 1 structure of conventional carry skip adder (CSKA)

Modified structure increases the speed but its power consumption is more than that of the conventional one. This difficulty is overcome by binary excess converter. In section 2 conventional carry skip adder is explained. Section 3 discusses about the modified carry skip adder (CI-CSKA).Section 4 discuss the implementation of binary excess converter in carry skip structure. Results and conclusion is given in section 5and 6.

2. CONVENTIONAL CARRY SKIP ADDER

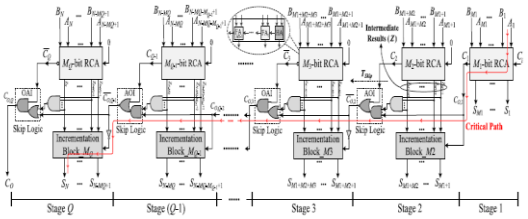
Structure of n-bit conventional carry skip adder (Conv-CSKA) is shown in the figure 1.Here only two stage is given, and it consist of ripple carry adder (RCA) block, multiplexer and some other basic gates. Here the RCA block consist of chain of full adders(FA) is used to perform the addition process. When we are giving n-bit input the RCA block perform the addition and producing sum and carry output. Here there are two input is arrived at the multiplexer logic, one is from the carry output of RCA block and another one is coming from the carry output of previous stage. Multiplexer is used to select one of the carry output among these two. Therefore 2 input multiplexer is used in the carry skip logic. Skip operation is performed using this multiplexer and gates shown in the figure. Pi is the propagation signal related to Ai and Bi .The product of propagation signal is used as selector signal of multiplexer. If the product of propagation signal is logic 0 the multiplexer will select the carry output of RCA block to next stage. If it is logic 1 the multiplexer select previous carry to the next stage. Thus the each stage of carry skip adder is depending on the previous stage.

The conv-CSKA may be implemented using fixed stage size (FSS) and variable stage size (VSS) where the highest speed may be obtained for the VSS structure.

3. MODIFIED CARRY SKIP ADDER(CI-CSKA)

The modified structure is known as CI-CSKA.As it is combining the concatenation and the incrementation schemes with the Conv-CSKA structure. The structure shown in figure 2 consist of RCA block , incrementation block and skip logic. Here the skip operation is performed by using the OAI-AOI gates. It provides us with the ability to use simpler carry skip logic. In conventional structure skip operation performed by 2:1 multiplexer and signal selecting gates. AOI-OAI gate require less number of transistor to perform the skip operation [7]. In this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, complement of carry is generated at the output of the skip logic of even stages. The propagation delay of modified structure is lower than that of the conventional carry skip adder. Note that the power consumption of the AOI or OAI gate count is smaller than that of the gate count of multiplexer but power consumption of the modified structure(CI-CSKA) is little more than that of conventional one. This is due to increase in the number of total gates.

Now describe the internal structure of CI-CSKA. The adder contains two N-bit input A and B, and Q stages. The given input may divided in to fixed stage size or variable stage size .The first stage consist of one block which is RCA block and the other stages consist of two blocks such as RCA block and incrementation block. The carry input of all the stages except first stage is given as zero. Thus when we are giving an input, all the RCA block produces their individual sum and carry output. since the carry input of each stage is zero simultaneous addition is takes place and each stage does not wait for the previous carry out .When the first block compute the summation of its corresponding input all other block compute the intermediate result . Note that the output of all RCA block except first block is called as intermediate result



because the actual carry is not

Fig.2 structure of modified carry skip adder (CI-CSKA)

added in this stage. We are just adding the carry input as zero for performing simultaneous operation. This is the concatenation process, therefore the obtained output of RCA block is not an actual result, thus it is mentioned as an intermediate result. The incrementation block is used to add the intermediate result with the carry output of previous stage. Incrementation block is a chain of full adder. The skip logic determine the carry output of next stage based on the intermediate result and carry output of previous stage as well as carry out of corresponding RCA block. If AOI gate is used in skip logic next skip logic should use OAI gates. These gates are alternatively used because of their inverting function. The critical path of CI-CSKA includes first RCA bloc k then all the skip logic and the last incrementation block. In the case of conventional carry skip adder critical path contain all RCA block and multiplexer logic. In CI-CSKA adder less number of gates are used in the critical path than the conventional one. Therefore the speed of addition is increased in modified structure.

4. BINARY TO EXCESS CONVERTER (BEC)

The CI-CSKA adder is efficient adder in terms of speed but the results shows that power consumption is increased due to increased number of total gates. In order to reduce the power consumption we are replacing some of the RCA block with binary to excess converter (BEC) [5].The main idea of this work is to use BEC instead of RCA with carry input =1

Fig.3 shows the structure of 4-bit binary to excess converter. It uses three EX-XOR gate, two AND gate and one NOT gate for 4-bit input. Similarly considering the case of RCA block, each RCA block is a chain of full adder and each of the full adder contain five gates. Addition of 4-bit input in a RCA block requires 4 full adder. since, one of the full adder contain five gates it require twenty gates for 4-bit addition .Note that in BEC using six gates for 4-bit addition where as in RCA uses

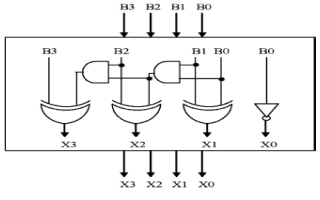


Fig.3 4-bit binary to excess converter

twenty gates for the addition of same bit. Therefore replacing the RCA with binary to excess converter (BEC) will reducing the total number of gates as well as power consumption. In our work we are replacing the RCA block with carry input as one of the CI-CSKA structure.

5. RESULTS

In this paper we are comparing the simulation result of CI-CSKA adder with the conventional carry skip adder. Table 1 shows the simulation results obtained by Xilinx software. It shows the gate count, delay and power of convention carry skip adder, CI-CSKA adder, CI-CSKA adder with BEC respectively. The main aim of this work is to increase the speed of conventional carry skip adder. From the table it is clear that the delay of conventional carry skip adder is 61.295ns and delay is 30.862ns for the CI-CSKA adder. Thus we can achieve the high speed by using the modified adder, which include concatenation and incrementation method for speeding up the operation and also it replaces the multiplexer logic with AOI-OAI gates. The power consumption of CI-CSKA adder is more than that of the conventional one. The power is about 990.73mw for C1-CSKA where as it is 807.38mw for conventional carry skip adder. This increased power consumption is due to increasing the number of total gate count. The power consumption of CI-CSKA adder is reduced by replacing its RCA block with binary to excess converter. Power consumption of CI-CSKA with BEC is reduced compare to the CI-CSKA. The power

TABLE 1 SIMULATION RESULTS

ADDERS	GATE COUNT	AY(ns)	OWER(mw)
Conventional carry skip adder(CSKA)	810	61.295	807.38
Modified adder (CI-CSKA)	684	30.862	990.73
CI-CSKA with BEC	681	31.043	974.36

consumption is reduced to 974.36 mw in BEC modification. Results shows that the delay is just increases from 30.862ns to 31.043ns.There is no huge variation in the delay and can reduce the power consumption in the case of CI-CSKA adder modified with binary to excess converter.

CONCLUSION

A simple approach is proposed in this paper to increase the speed of conventional carry skip adder. The speed enhancement is achieved by modifying the structure through concatenation and incrementation technique also replacing the multiplexer logic with low power gates such as AOI-OAI. The simulation result shows that the delay of modified adder (CI-CSKA) is reduced compared to the conventional structure. The results also suggested that the CI-CSKA structure is a very good adder for high speed application. The major drawback of this adder is the increased power consumption which is overcome by replacing some of the RCA block with binary to excess converter (BEC).The proposed CI-CSKA adder with BEC is an efficient adder in terms of speed and power consumption.

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