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Floating Point Adder with Pipelining Using VHDL

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Abstract— Floating Point arithmetic is by far the most used way of approximating real number arithmetic for performing numerical calculations on modern computers. Each computer had a different arithmetic for long time: bases, significant and exponents' sizes, formats, etc. Each company implemented its own model and it hindered the portability between different equipments until IEEE 754 standard appeared defining a single and universal standard. The aim of this project is implementing a floating point adder with pipelining according with the IEEE 754 standard and using the hardware programming language VHDL, which results in reduced processing time, reduced system delay, increased efficiency with accuracy.

Index Terms—Floating point adder, VHDL ,Pipelining technique, Adder

1INTRODUCTION

Floating-point adders are critically important components in modern microprocessors and digital signal processors. The architectures developed so

far for floating point adders are based on sequence of significant operations: Swap, shift, add, normalize and round. Due to these operations, the overall process of addition slows down. Floating-point adders must be fast to match with the increasing clock rates demanded by deep sub-micron technologies; also they must be small for being used in parallel processing systems. Since, in the traditional adders, all the stages were performed with single clock cycle, but the frequency of this clock was restricted due to the circuit constraints. Hence, whenever, the addition of a large number of values was performed, the traditional floating-point adders proved to be inefficient. This latency could be overcome if the concept of pipelining in the simple adder is introduced.

The floating- point adder had been subdivided into four stages, which were pipelined according to the proper timing sequences. The clock frequency, which could be used for these stages, could be higher as compared to the clock frequency used for traditional floating- point adder. Also, while the two inputs are being processed and passed on to subsequent stages, new inputs enter the initial stage and the cycle continues. This results in overall faster operation. In this paper, the floating-point algorithm is explained and floating point adder implementation using Very Large Scale Integration Hardware Descriptive Language (VHDL) is described. It further deals with the concept of pipelining and the enhanced capability of the floating- point adder. Simple floating-point adder and pipelined adder have been compared in terms of speed of operation and area on chip.

SINGLE PRECISION FLOATING POINT REPRESENTATION

The IEEE single precision floating point standard representation requires a 32 bit word, which may be represented from 0 to 31, left to right. The first bit is the sign bit, s, the next eight bits are the exponent bits, 'E', and the final 23 bits are the fraction 'F':

S EEEEEEEE FFFFFFFFFFFFFFFFFFFFF

0 1 8 9 31

FLOATING POINT NUMBERS

The floating point numbers representation is based on the scientific notation: thedecimal point is not set in a fixed position in the bit sequence, but its position isindicated as a base power.

All the floating point numbers are composed by three components:

- *Sign:* it indicates the sign of the number (0 positive and 1 negative)

- *Mantissa*: it sets the value of the number
- *Exponent*: it contains the value of the base power (biased)
- *Base*: the base (or radix) is implied and it is common to all the numbers (2 for binary numbers)

The free using of this format caused either designed their own floating pointSystem. For example, Konrad Zuse did the first modern implementation of afloating point arithmetic in a computer he had built (the Z3) using a radix-2number system with 14-bit significant, 7-bit exponents and 1-bit sign. On theother hand the PDP-10 or the Burroughs 570 used a radix-8 and the IBM 360had radix-16 floating point arithmetic.This led to the need for a standard which would make a clear and concise format to be used by all the developers.

FLOATING POINT ALGORITHM

The floating-point representation of a numberincludes three fields: Sign bit (Si,), exponent (Ei,) andthe mantissa (Fi). The algorithm for floating pointaddition/subtraction consists of the following steps:(i) Load the inputs and check for exceptional inputs(NaNs, infinity and zero); (ii) Align the mantissas(right shift the significant of the smaller operand); (iii)

Add or subtract the mantissas; and (iv) Normalize theresults and generate the exceptions.

PIPELINING TECHNIQUE

Pipelining, a technique for achieving faster clockrates while sacrificing latency, offers an economicway to realize temporal parallelism in digital systems.To achieve pipelining, input process must besubdivided into a sequence of subtasks, each of whichcan be executed by specialized hardware stage thatoperates concurrently with other stages in thepipeline. The adder design pipelines the steps,comparing, swapping, shifting, addition, andnormalization, to achieve a summation every clock cycle. Each pipeline stage performs operationsindependent of others. Input data to the addercontinuously streams in.

IMPLEMENTING PIPELINING IN ADDER THROUGH VHDL

The various VHDL constructs used in addition tothe very elementary ones are: Package, procedure,function and port mapping. A floating-point value, N,can be represented as

$N=S \times R^E$

Where S is a fixed value multiplied by a radix, R, tosome power E.

The algorithm to add two numbers with thisrepresentation requires that the radix power E, be thesame in power and sign. If so, the significantcomponents, S, can be summed together whilekeeping the same radix to some power E, as themultiplier. If they are not same, adjustment of thesignificant is one prior to addition.

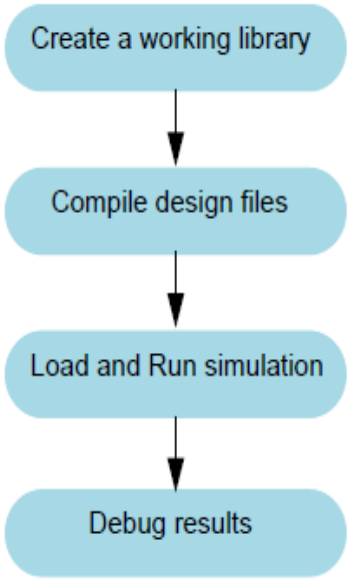
PROPOSED SYSTEM

In this project we are implementing a design that serves as a Floating Point Adder with pipelining. This system is designed to eliminate the time delay present in the earlier existing systems and will be working on the enhancement of the output values and ensuring that the system is accurate to 100% in delivering the output.

This is achieved by implementing the pipelining directly inside the adder which will eliminate the number of cycles used for the processing of the data and also helps in reducing the time taken to perform an operation widely throughout the system.

SOFTWARE DESCRIPTION

MODELSIM

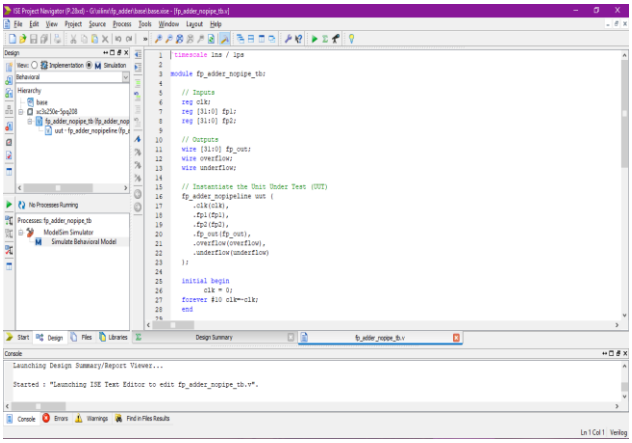


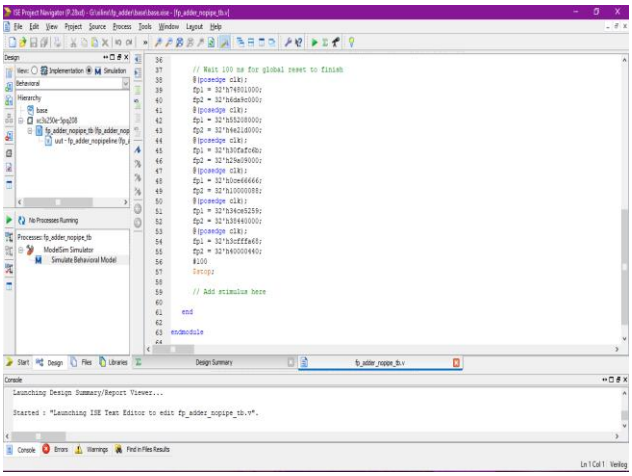
Basic simulation flow

Modelsim is a hardware simulationand debug environment primarily targeted at smaller ASIC and FPGA design. Modelsim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Modelsim is easy to use. The unified debug and simulation environment provide today's FPGA designers the advanced capabilitiesmake their work productive. Modelsim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language designs.

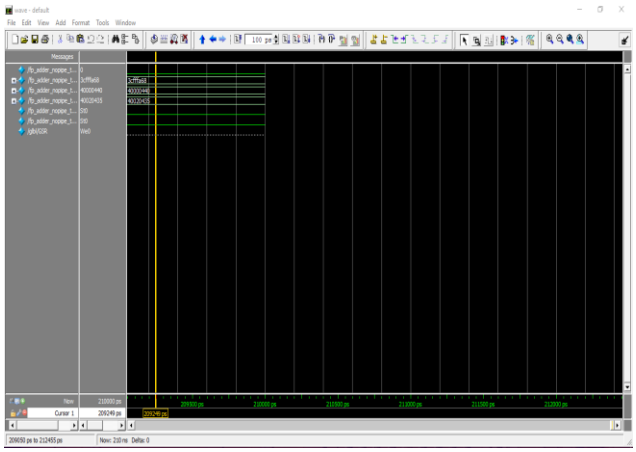
RESULT AND DISCUSSION

The snapshot of the program is shown below





And the output obtained is shown below



REFERENCES

[1] P. Bannon et al. Internal architecture of Alpha 21164 microprocessor. COMPCON 95, pages 79{March 1995}.

[2] B. J. Benschneider et al. A pipelined 50-Mhz CMOS 64-bit floating-point arithmetic

Processor. IEEE Transactions on Computers, 24(5):1317{1323, October 1989}.

[3] M. Birman, A. Samuels, G. Chu, T. Chuk, L. Hu, J. McLeod, and J. Barnes. Developingthe WTL 3170/3171 Sparc floating-point co-processors. IEEE Micro{63,February 1990}.

[4] D. Greenley et al. UltraSPARC: the next generation superscalar 64-bit SPARC,1995.

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