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An Efficient Design of Low power Baugh Wooley Multiplier with Carry Save Adder for DSP Applications

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Abstract- In this paper we have proposed Baugh Wooley Multiplier with carry skip adder. Baugh Wooley multiplier performs an multiplication operation on signed numbers only. Most signal processing application performs truncated multiplication in order to decrease the word size. When direct truncation is used it provides significant savings in power, area, complexity and timing it can also introduces large amount of error in the output. so here in this paper a programmable truncated Baugh Woolley multiplier to enhance the speed and to reduce the critical path delay. The proposed work designed on 8 bit and 16 bit and study also shows the comparison between carry save adder and redesigned the carry skip adder using Baugh Woolley multiplier having reduced area, power and delay. The Carry Save Adder (CSA) tree and the Carry skip (CSA) adder used to reduce the power consumption compared to conventional one multiplier operation. Since signed multiplication operation is performed by the same multiplier unit and the area reduces the multiplier complexity and also less power and which is analyzed in in Xilinx ISE 14.2 i.

Index Terms— Digital signal processing (DSP), fault tolerant, low power, carry save adder, carry skip adder, truncatedmultiplication.

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I. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact implementation. The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To achieve speed improvements Baugh-Wooley algorithm can be used.Truncated multiplication has been widely studied by means of achieving both power and area improvements in the field of an arithmetic circuit design, at the expense of signal degradation [6]–[12]. As the truncated multipliers are smaller than full-precision ones, they not only achieve their improvements in power consumption and area, but result in different timing distributions. The existence of an synergic benefits derived from the combination of truncated multiplication and VOS using an fault tolerance strategy is presented in this brief where both techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) structure

This brief is organized as an follows. Section II reviews some of the latest relevant VOS, fault tolerance and truncated multiplication advances. Section III details and an programmable truncated multiply-and-accumulate (PTMAC) architecture used in this brief. The proposed implementation, where fault tolerance and programmable truncation are combined, is analyzed in Section IV.

2.EXISTING WORK

Baugh-Wooley multiplier of an Two's compliment Signed multipliers is an well known algorithm for signed multiplication because it maximizes their regularity of the multiplier and allows all partial products must have positive sign bits [3]. Baugh–Wooley technique was developed to

design an direct multipliers for two's compliment numbers [9]. When multiplying two's compliment numbers directly, each of the partial products to be added is a signed numbers. Thus both partial product has to be sign extended to the width of the final product in order to form a exact sum by the Carry Save Adder (CSA) tree. According to Baugh-Woolley approach, an efficient method of adding extra entries to the bit matrix recommended to avoid having deal with the negatively weighted bits in the partial product matrix. The Baugh Woolley algorithm is a relative straightforward way of performing signed multiplications. Demonstrates the algorithm for an 8-bit case, where the partial product array has been reorganized according to the scheme of Hatamian.

The formation of the reorganized partial-product array comprises three steps: i)the most important partial product of the first N-1 rows and the last row of partial products except the most significant have to be canceled, ii) a constant one is added to the Nth column, iii) the most significant bit (MSB) of the final result is canceled. Multiplication involves two basic operations: the generation of the partial product and their accumulation. Therefore, there are Possible approaches to speed up the multiplication reduces the complexity, and as a result reduces the time needed to accumulate the partial products. Both answers can be applied simultaneously.

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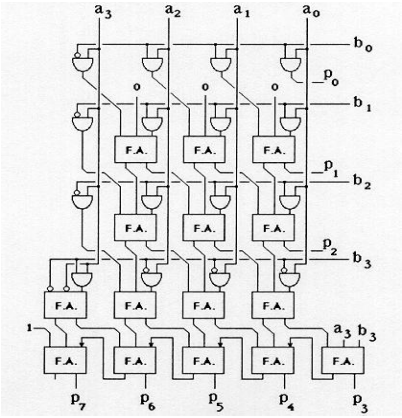

Fig 1.1 Block diagram of a 4*4 Baugh-Wooley multiplier

B. 8 BIT BAUGH WOOLEY MULTIPLIER

It is an efficient way to handle the sign bit. Baugh Wooley multiplier uses only full adders. All bit products are produced in parallel & collected through an array of full adder & final Carry Save Adder (CSA). The creation of the reorganized partial-product array comprises three steps:

i) The most significant bit (MSB) of the first N-1partial-product rows and all bits of the last partial product row, except its MSB, are inverted.

ii) A '1' is added to the nth column.

iii)The MSB of the final result is negated

The least-significant columns of Baugh-Wooley multiplier is truncated to yield the 8-bit output in 8×8 multiplier. The uniform quantization scheme is applied to both signed multiplier and Baugh-Wooley multiplier to reduce the partial-products in uniform quantization scheme some of the coefficients of the partial products are quantized with two bits, while the remaining coefficients are quantized with single bit.

Multiplication involves 2 basic operations: the generation of the partial product and their accumulation .Therefore, there are possible approaches to speed up the multiplication decreases the complexity, and as a result decreases the time needed to accumulate the partial products Both answers can be applied simultaneously.

Multipliers are, in cause, complex adder arrays represents a 16x16-bit BW multiplier a BW multiplier is a regular multiplier that is well-suited for 2's-complement numbers Multiplication is done in two steps. First the partial products are computed from the logical AND of the multiplicand A and a multiplier bit Bi the second step accumulates the partial products and accumulation is done after every partial product generation by arrays of adders every box is correspond to an AND gate, followed by an 1-bit transmission-gate Full-adder the last row is essentially for an N-bit Full-adder (in this case, N is equal to 16), which combines all the partial product results.

The critical path for the BW multiplier is the delay of the longest vertical chain of adders and the last row of adders the last row can be reduced by implement an N-bit Carry-Save Adder for the case of a 16x16-bit Baugh-Wooley Multiplier, power and delay should be proportional to the required precision bits of the output the worst-case power consumption will takes place when the required input precision is 16 bits and the best-case consumption will be when the input precision is 1 bit.

3.TRUNCATED MULTIPLICATION

In systems where it is not necessary to compute the exact least significant part of the product, truncated multipliers allow power, area, and timing improvements by skipping the implementation of sections of the least significant part of the partial product matrix. Instead of computing the full-precision output, the output is from the sum of the first (N + h) columns (where $0 \leq h \leq N$), where N is the operand width, addition to that an estimation of the erased bits

In many applications, product values produced by fixed width N × N bit multipliers are truncated or rounded back to the original bit width in latter stages of the algorithm flow. Truncation permits a method of reducing the complexity of the multiplier unit by replacing the lower parts of the partial product matrix by a smaller compensation circuit, and its variants range from very aggressively truncated applications [6], [12] to faithfully rounded truncated multipliers [16], [17].

4.CONVENTIONAL MAC UNIT

MAC are the building blocks of the processor and has a great impact on the speed of processor.MAC is composed of adder, multiplier and an accumulator. The inputs for the MAC are to be fetched from memory location and fed to multiplier block of MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location.

MAC mainly consist two parts

- Multiplier
- Accumulator.

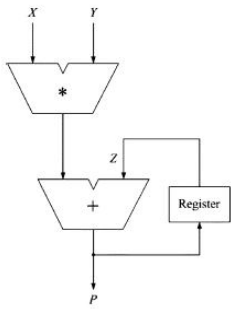

Figure 1.2 Basic Architecture of MAC Unit

In computing, especially digital signal processing, the multiply accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier accumulator (MAC, or MAC unit); the operation itselfis also often called a MAC or a MAC operation [1].Refer to (2) the MAC operation modifies an accumulator.

5. CARRY SAVE ADDER

In Carry Save Adder (CSA), three bits are added parallel at a time. In this method, the carry is not propagated through the stages. Instead, carry is stored in present stage, and updated as addend value in their next stage. Hence, the delay due to the carry is reduced in this scheme.

6. CARRY SKIP ADDER

Multiplication is widely required in digital signal processing. Parallel multipliers provide a high-speed method for multiplication, but require larger area for their VLSI implementations. Thus an important design goal is to reduce the area requirement of the rounded bit output multiplier. This paper presents a method for baugh-wooley multiplication which computes the products of two n-bit numbers and truncates the lower bits using truncation control bits. Truncated multipliers can be used in finite impulse response (FIR) filters and discrete cosine transforms (DCT). The truncated multiplier shows much more reduction in area as compared to standard multiplier. Based on this paper the modification done on the multiplier. The proposed work should be high speed Baugh Woolley multiplier with programmable truncation.

In this paper the modification should be planned to done using high speed baugh-woolley multiplier with programmable truncation. Multiplication is an main basic function in arithmetic functions. Multiplication-based functions such as Multiply and Accumulate (MAC) unit and inner product are among some of the mostly used Computation.

As the name specifies, Carry Skip Adder (CSkA) utilize skip logic in their propagation of carry [1]. It is designed to speed up the addition process by adding a propagation of carry bit around a portion of whole adder.

7. RESULTS

The design is developed using in VHDL and then synthesized and simulated using Xilinx ISE 14.2i. And Power Calculations have found for MAC Unit using Xilinx Analyze PowerX a Multiplier is designed Baugh wolley Multiplier and with two adders using Carry Save Adder and carry skip adder Area, Power and Delay results are Present Below. While compared to carry save adder its produces low complexity, area and power.

8 BIT BAUGH WOOLEY MULTIPLIER:

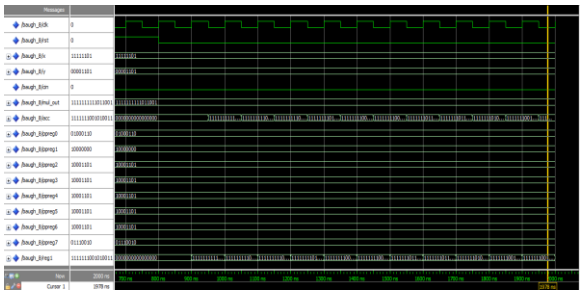

Figure 1.3 Simulation Result of 8*8 Bit MAC Multiplier

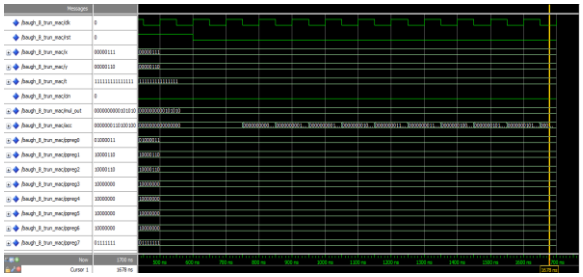

Figure 1.4 Simulation Result of 8*8 Bit Truncated MAC Multiplier

16 BIT BAUGH WOOLEY MULTIPLIER:

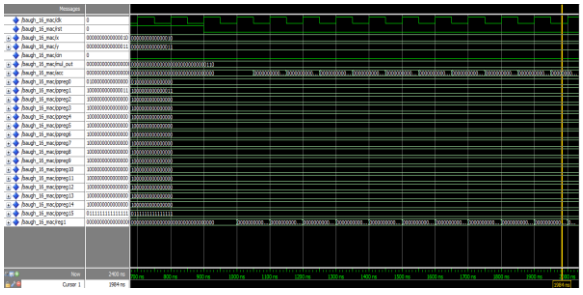

Figure 1.5 Simulation Result of 16*16 Bit MAC Multiplier

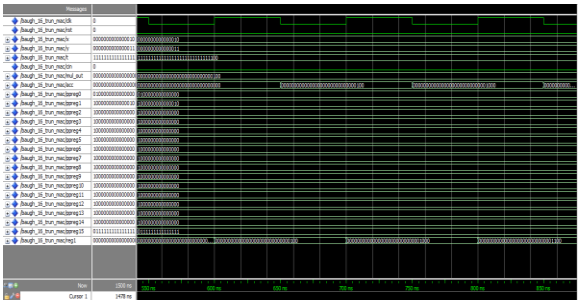

Figure 1.6 Simulation Result of16*16 Bit MAC Multiplier

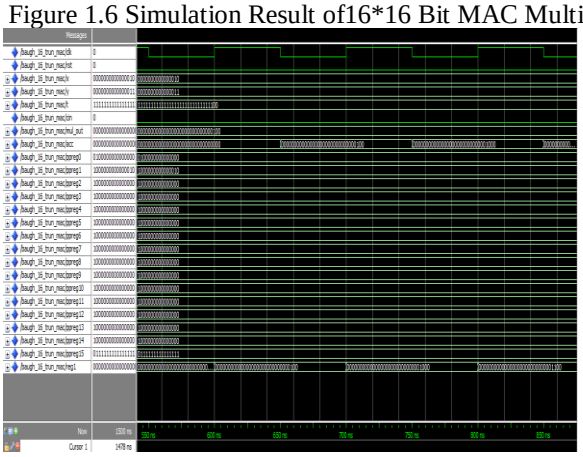

Figure 1.7 Simulation Result of16*16Bit Truncated MAC Multiplier

TABLE I. Comparison of 8*8 and 16*16 Bit Multiplier

h-Wooley tiplier	**Y(ns)**	**A (µm)**	**ER (mW)**
Bit MAC	**790** **790**	**568** **568**	**360** **436**
Truncated MAC	**511**	**770**	**394**
it MAC	**305**	**585**	**202**
save adder		**.62**	**0.48**
ry skip dder	**08**	**.63**	**2.54**

CONCLUSION

Here, we proposed a noval design for baugh wooley multiplier using carry save adder and carry skip adder .Also the proposed design by using carry skip adder is used here for the fast addition and proved and delay ,power will be reduced to conventional carry save adder.

In these proposed method, the attractive features of the carry skip adder structure can be focused on to reduce the multiplier delay by modifying partial product reduction path. A carry skip adder (CSKA) structure that has a higher speed yet lower power consumption compared with the conventional one. This modification for carry skip adder increases the speed considerably while maintaining the low area and power consumption features of the CSKA.

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